LP8755 Multi-Phase Six-Core Step-Down Converter

Check for Samples: LP8755

1 Features

- Six High-Efficiency Step-Down DC-DC Converter Cores:
  - Max Output Current 15 A
  - Cores Bundled to a 6-Phase Converter
  - Load Current Reporting
  - Programmable Overcurrent Protection (OCP)
  - Auto PWM/PFM and Forced-PWM Operations and Automatic Low Power-Mode Setting
  - Automatic Phase Adding/Shedding
  - Remote Differential Feedback Voltage Sensing
  - Output Voltage Ramp Control
  - V_{OUT} Range = 0.6 V to 1.67 V
- I^2C-Compatible Interface which Supports Standard (100 kHz), Fast (400 kHz), and High-Speed (3.4 MHz) Modes
- Four Selectable I^2C Addresses
- Interrupt Function with Programmable Masking
- Output Short-Circuit and Input Overvoltage Protection (OVP)
- Spread Spectrum and Phase Control for EMI Reduction
- Overtemperature Protection (OTP)
- Undervoltage Lockout (UVLO)

2 Applications

- Smart Phones, eBooks and Tablets
- GSM, GPRS, EDGE, LTE, CDMA and WCDMA Handsets
- Gaming Devices

3 Description

The LP8755 is designed to meet the power management requirements of the latest applications processors in mobile phones and similar portable applications. The device contains six step-down DC-DC converter cores, which are bundled together in a 6-phase buck converter. The device is fully controlled by a SmartReflex™-compatible (DVS) interface or an I^2C-compatible serial interface.

The automatic PWM/PFM operation together with the automatic phase adding/shedding maximizes efficiency over a wide output current range. The LP8755 supports remote differential voltage sensing to compensate IR drop between the regulator output and the point-of-load thus improving the accuracy of the output voltage.

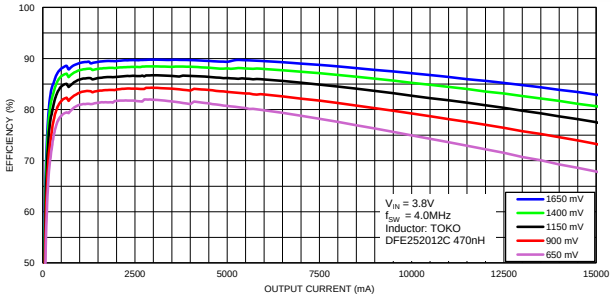
The protection features include short-circuit protection, current limits, input OVP, UVLO, temperature warning, and shutdown functions. Several error flags are provided for status information of the IC. In addition, I^2C read-back includes total load current and load current for each buck core: The LP8755 has the ability to sense current being delivered to the load without the addition of current sense resistors. During start-up, the device controls the output voltage slew rate to minimize overshoot and the inrush current.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LP8755	DSBGA (49)	3.022 mm x 2.882 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Efficiency vs. Load Current



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4 Revision History

Changes from Original (November 2013) to Revision A	Page
• Changed formatting to match new TI datasheet guidelines; added *Device Information* and *ESD Ratings* tables, *Power Supply Recommendations, Layout, and Device and Documentation Support* sections; moved some curves to *Application Curves* section, reformatted *Detailed Description* and *Application and Implementation* sections, adding additional content.	1

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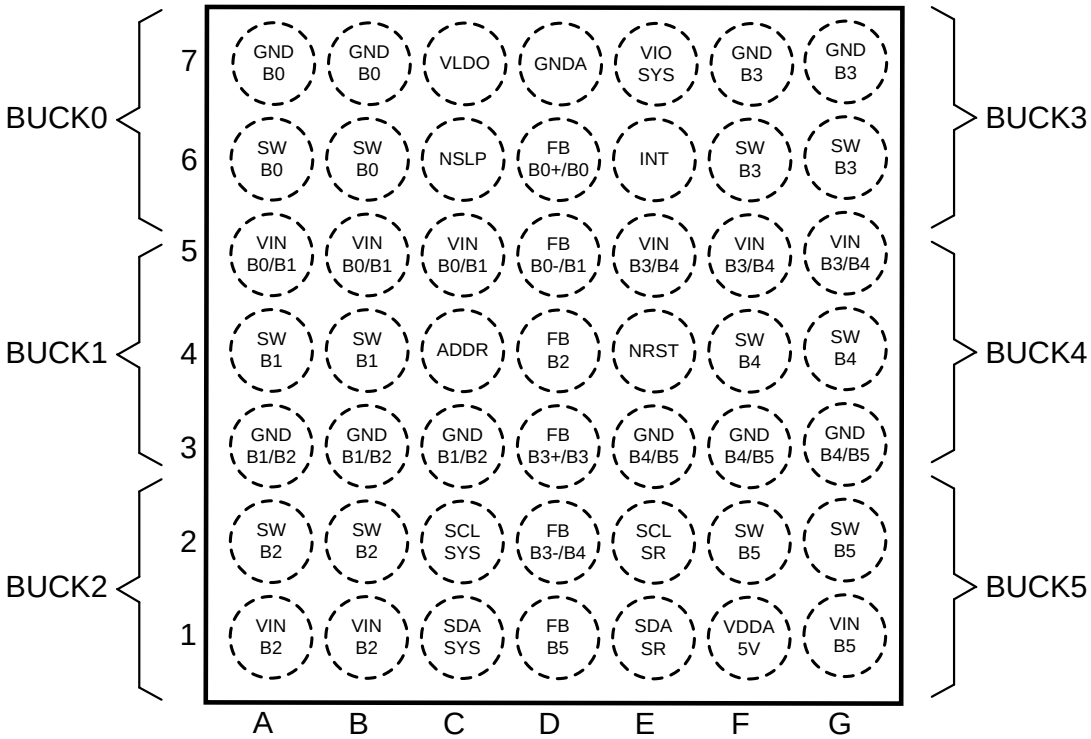
5 Pin Configuration and Functions

DSBGA (YFQ)
49 Pins
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
A1, B1	VINB2	P	Input for Buck 2. The separate power pins VINBXX are not connected together internally - VINBXX pins must be connected together in the application and be locally bypassed.
A2, B2	SWB2	A	Buck 2 switch node
A3, B3, C3	GNDB1/B2	G	Power Ground for Buck 1 and Buck 2
A4, B4	SWB1	A	Buck 1 switch node
A5, B5, C5	VINB0/B1	P	Input for Buck 0 and Buck 1. The separate power pins VINBXX are not connected together internally - VINBXX pins must be connected together in the application and be locally bypassed.
A6, B6	SWB0	A	Buck 0 switch node
A7, B7	GNDB0	G	Power Ground for Buck 0
C1	SDASYS	D/I/O	Serial interface data input and output for system access. Connect a pullup resistor.
C2	SCLSYS	D/I	Serial interface clock input for system access. Connect a pullup resistor.
C4	ADDR	D/I	Serial bus address selection. Connect to GND (addr = 60h), VIOSYS (addr = 61h), SDASYS (addr = 62h) or SCLSYS (addr = 63h).
C6	NSLP	D/I	Full Power to Low Power state transition control signal (By default active LOW for Low-Power PFM mode)
C7	VLDO	A	Internal supply voltage capacitor pin. A ceramic low ESR 1-µF capacitor should be connected from this pin to GNDA. The LDO voltage is generated internally, do NOT supply or load this pin externally.
D1	FBB5	A	Not used for six-phase converter. Connect to GND.
D2	FBB3−/B4	A	Not used for six-phase converter. Connect to GND.
D3	FBB3+/B3	A	Not used for six-phase converter. Connect to GND.
D4	FBB2	A	Not used for six-phase converter. Connect to GND.

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
D5	FBB0−/B1	A	Remote sensing (negative). Connect to the respective sense pin of the processor or to the negative power supply trace of the processor as close as possible to the processor.
D6	FBB0+/B0	A	Remote sensing (positive). Connect to the respective sense pin of the processor or to the positive power supply trace of the processor as close as possible to the processor.
D7	GNDA	G	Ground
E1	SDASR	D/I/O	Serial Interface data input and output for Dynamic Voltage Scaling (DVS). Connect a pullup resistor / connect to GND if not used.
E2	SCLSR	D/I	Serial Interface clock input for DVS. Connect a pullup resistor / connect to GND if not used.
E3, F3, G3	GNDB4/B5	G	Power Ground for Buck 4 and Buck 5
E4	NRST	A	Voltage reference input for DVS interface. Setting NRST input HIGH triggers start-up sequence.
E5, F5, G5	VINB3/B4	P	Input for Buck 3 and Buck 4.The separate power pins VINBXX are not connected together internally - VINBXX pins must be connected together in the application and be locally bypassed.
E6	INT	D/O	Open-drain interrupt output. Active LOW. Connect a pullup resistor to I/O supply.
E7	VIOSYS	A	This pin shall be tied to the system I/O-voltage. Bias supply voltage for the device. Enables the I/O interface: All registers are accessible via serial bus interface when this pin is pulled high. An internal power-on reset (POR) occurs when VIOSYS is toggled low/high. The I^2C host should allow at least 500 µs before sending data to the LP8755 after the rising edge of the VIOSYS line.
F1	VDDA5V	P	Input for Analog blocks
F2, G2	SWB5	A	Buck 5 switch node
F4, G4	SWB4	A	Buck 4 switch node
F6, G6	SWB3	A	Buck 3 switch node
F7, G7	GNDB3	G	Power Ground for Buck 3
G1	VINB5	P	Input for Buck 5. The separate power pins VINBXX are not connected together internally - VINBXX pins must be connected together in the application and be locally bypassed.
A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin			

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
INPUT VOLTAGE			
Voltage on power connections (VIOSYS, VDDA5V, VINBXX)	−0.3	6	V
Voltage on logic pins (input or output pins) (SCLSYS, SDASYS, NRST, NSLP, ADDR, INT, SCLSR, SDASR)	−0.3	6	
Buck switch nodes (SWBXX)	−0.3	(V_{VINBXX} + 0.2 V) with 6 V max	V
VLDO, FBB0+/B0, FBB0−/B1, FBB2, FBB3+/B3, FBB3−/B4, FBB5	−0.3	2	V
All other analog pins	−0.3	6	
TEMPERATURE			
Junction temperature (T_{J-MAX})		150	°C
Maximum lead temperature (soldering, 10 s)[3]		260	
Storage temperature, T_{stg}	−65	150	

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) All voltage values are with respect to network ground pin.
(3) For detailed soldering specifications and information, please refer to Texas Instruments AN-1112: *DSBGA Wafer-Level Chip-Scale Package* (SNVA009).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
INPUT VOLTAGE			
Voltage on power connections (VDDA5V, VINBXX)	2.5	5	V
Voltage on VIOSYS	1.8	smaller of 3.3 V or V_{VINBXX}	V
SCLSYS, SDASYS, ADDR	0	V_{VIOSYS}	V
SCLSR, SDASR, NSLP, INT	0	V_{NRST}	V
NRST	0	1.8	V
TEMPERATURE			
Junction temperature (T_J)	−40	125	°C
Ambient temperature (T_A)[3]	−40	85	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) All voltage values are with respect to network ground pin.
(3) Junction-to-ambient thermal resistance value given is valid for High-K PCB, and is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

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6.4 Thermal Information

THERMAL METRIC[1]		LP8755 YFQ 49 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	49.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance[3]	0.2	
$R_{\theta JB}$	Junction-to-board thermal resistance[4]	6.6	
ψ_{JT}	Junction-to-top characterization parameter[5]	2.9	
ψ_{JB}	Junction-to-board characterization parameter[6]	6.5	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance[7]	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψJT, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψJB, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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6.5 General Electrical Characteristics

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range –40°C ≤ T_A ≤ 85°C; typical (TYP) values at T_A = 25°C (unless otherwise noted). V_{VDDA5V} = V_{VINBXX} = 3.7 V, V_{VIOSYS} = V_{NRST} = 1.8 V, V_{OUT} = 1.1 V (unless otherwise noted).(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENTS						
I_{SHDN}	Shutdown supply current. Total current into power connections VDDA5V and VINBXX	V_{VIOSYS} = 0 V, V_{NRST} = 0 V		0.1	2	µA
I_{STBY}	Standby mode supply current. Total current into power connections VDDA5V and VINBXX	V_{VIOSYS} = 1.8 V, V_{NRST} = 0 V		80		µA
I_{Active}	Active mode current consumption. Total current into power connections VDDA5V and VINBXX	PFM Mode, no load, one core active		0.4		mA
		Forced PWM Mode, no load, one core active		14.5		mA
LOGIC AND CONTROL INPUTS SCLSYS, SDASYS, ADDR						
V_{IL}	Input low level	V_{VIOSYS} = 1.8 V to 3.3 V			0.3 x V_{VIOSYS}	V
V_{IH}	Input high level	V_{VIOSYS} = 1.8 V to 3.3 V	0.7 x V_{VIOSYS}			V
V_{hys}	Hysteresis of Schmitt trigger inputs (SCLSYS, SDASYS)		0.1 x V_{VIOSYS}			V
C_i	Capacitance of pins	See(3)			4	pF
LOGIC AND CONTROL INPUTS SCLSR, SDASR, NSLP, NRST						
V_{IL}	Input low level	V_{NRST} = 1.8 V			0.3 x V_{NRST}	V
V_{IH}	Input high level	V_{NRST} = 1.8 V	0.7 x V_{NRST}			V
V_{hys}	Hysteresis of Schmitt trigger inputs (SCLSR, SDASR)		0.1 x V_{NRST}			V
C_i	Capacitance of SCLSR and SDASR pins				4	pF
R_{IN}	Input resistance	NRST pulldown resistor to GND		1200		kΩ
V_{IL_NRST}	Input low level NRST				0.54	V
V_{IH_NRST}	Input high level NRST		1.3			V
LOGIC AND CONTROL OUTPUTS						
V_{OL}	Output low level	Voltage on INT pin, I_{SINK} = 3 mA, V_{NRST} = V_{VIOSYS} = 1.8 V			0.4	V
		Voltage on SDASYS, SDASR, I_{SINK} = 3 mA, V_{NRST} = V_{VIOSYS} = 1.8 V			0.36	V
R_P	External pullup resistor for INT	To I/O Supply		10		kΩ
ALL LOGIC AND CONTROL INPUTS						
I_{LEAK}	Input current	All logic inputs over pin voltage range. Note that NRST pin does have an 1.2-MΩ internal pulldown resistor and current through this resistor is not included into I_{LEAK} rating. T_A = 25°C	−1		1	µA

(1) All voltage values are with respect to network ground pin.
(2) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis. Typical (Typ.) numbers are not ensured, but do represent the most likely norm.
(3) Maximum capacitance of SCLSYS or SDASYS line is 8 pF, if ADDR pin is connected to line for serial bus address selection.

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6.6 6-Phase Buck Electrical Characteristics

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range –40°C ≤ T_A ≤ 85°C; typical (TYP) values at T_A = 25°C (unless otherwise noted)(1)(2). V_{VDDA5V} = V_{VINBXX} = 3.7 V, V_{VIOSYS} = V_{NRST} = 1.8 V, V_{OUT} = 1.1 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Differential feedback voltage(3)(4) $V_{FB0+/B0}$ - $V_{FB0-/B1}$	PWM Mode, V_{OUTSET} = 0.6 V to 1.67 V, I_{OUT} ≤ 15 A(5)	0.975 x V_{OUTSET}	V_{OUTSET}	1.025 x V_{OUTSET}	V
		PFM Mode, V_{OUTSET} = 0.6 V to 1.67 V, I_{OUT} ≤ 375 mA	0.975 x V_{OUTSET}	V_{OUTSET}	1.025 x V_{OUTSET}	
		Low-Power PFM Mode, V_{OUTSET} = 0.6 V to 1.67 V, I_{OUT} ≤ 30 mA	0.97 x V_{OUTSET}	V_{OUTSET}	1.03 x V_{OUTSET}	
I_{LIMITP}	High side switch current limit	3-A register setting(4)	2700	3200	3700	mA
I_{LIMITN}	Low side switch current limit	Reverse current(4)	650	850	1050	
V_{OUT}	Output voltage	Range, programmable by register setting	0.6		1.67	V
		Step		10		mV
f_{SW}	Switching frequency	2.5 V ≤ V_{VINBXX} ≤ 5 V, 0.6 V ≤ V_{OUTSET} < 0.8 V (4)	2.7	3	3.4	MHz
		2.5 V ≤ V_{VINBXX} ≤ 5 V, 0.8 V ≤ V_{OUTSET} ≤ 1.67 V (4)	3.6	4	4.5	
R_{DSON_P}	Pin-pin resistance for PFET	Test current = 200 mA; Split FET		120		mΩ
		Test current = 200 mA; Full FET		60		
R_{DSON_N}	Pin-pin resistance for NFET	I_{OUT} = –200 mA		50		
I_{LK_HS}	High-side leakage current	V_{SW} = 0 V, Per Buck Core			2	µA
I_{LK_LS}	Low-side leakage current	V_{SW} = 3.7 V = V_{VINBXX}, per buck core			2	
R_{PD}	Pull-down resistor	Enabled via control register, Active only when converter disabled, Per Buck Core		250		Ω
R_{IN_FB}	Differential feedback Input resistance(6)	T_A = 25°C	200	300	400	kΩ

(1) Junction-to-ambient thermal resistance value given is valid for High-K PCB, and is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(2) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics. The performance of the LP8755 device depends greatly on the care taken in designing the Printed Wiring Board (PWB). The use of low inductance and low serial resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the IC and between the power and ground pins to support high peak currents being drawn from System Power Rail during turn-on of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance and capacitance can easily become the performance limiting items.
(3) Due to the nature of the converter operating in PFM Mode/Low-Power Mode, the feedback voltage accuracy specification is for the lower point of the ripple. Thus the converter will position the average output voltage typically slightly above the nominal PWM-Mode output voltage.
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(5) The power switches in the LP8755 are designed to operate continuously with currents up to the switch current limit thresholds. However, when continuously operating at high current levels there will be significant heat generated within the IC and thus sustained total DC current which the device can support is typically limited by thermal constraints. Thermal issues will become extremely important when designing PCB and the thermal environment of the LP8755. PCB with high thermal efficiency is required to ensure the junction temperature is kept below 125°C. Completing thermal analyses in early stages of the product design process is highly recommended to predict thermal performance at board level. Under high current load conditions the serial bus master device must monitor the temperature of the converter using the Thermal warning feature, see *Protection Features Characteristics*. If the 2nd thermal warning is triggered at 120°C, the application must quickly decrease the load current to keep the converter within its recommended operating temperature.
(6) Datasheet min/max specification limits are specified by design.

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6.7 6-Phase Buck System Characteristics

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range –40°C ≤ T_A ≤ 85°C; typical (TYP) values at T_A = 25°C (unless otherwise noted)(1)(2). V_{VDDA5V} = V_{VINBXX} = 3.7 V, V_{VIOSYS} = V_{NRST} = 1.8 V, V_{OUT} = 1.1 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{RAMP}	Ramp timer	Programmable via control register(3)				mV/µs
		RAMP_B0[2:0] = 000		30		
		RAMP_B0[2:0] = 001		15		
		RAMP_B0[2:0] = 010		7.5		
		RAMP_B0[2:0] = 011		3.8		
		RAMP_B0[2:0] = 100		1.9		
		RAMP_B0[2:0] = 101		0.94		
		RAMP_B0[2:0] = 110		0.47		
		RAMP_B0[2:0] = 111		0.23		
T_{START}	Start-up time	Time from NRST-HIGH to start of switching		25		µs
T_{RAMP}	V_{OUT} rise time	Time to ramp from 5% to 95% of V_{OUT}		20		µs
$I_{PFM–PWM}$	PFM-to-PWM switch–over current threshold	Average output current, programmable via control register, V_{OUT} = 1.1 V. (4)				mA
		PFM_EXIT_B0[2:0] = 000		100		
		PFM_EXIT_B0[2:0] = 001		125		
		PFM_EXIT_B0[2:0] = 010		150		
		PFM_EXIT_B0[2:0] = 011		175		
		PFM_EXIT_B0[2:0] = 100		225		
		PFM_EXIT_B0[2:0] = 101		275		
		PFM_EXIT_B0[2:0] = 110		325		
		PFM_EXIT_B0[2:0] = 111		375		
$I_{PWM–PFM}$	PWM-to-PFM switchover current threshold	Average output current, programmable via control register, V_{OUT} = 1.1 V. (4)				mA
		PFM_ENTRY_B0[2:0] = 000		50		
		PFM_ENTRY_B0[2:0] = 001		75		
		PFM_ENTRY_B0[2:0] = 010		100		
		PFM_ENTRY_B0[2:0] = 011		125		
		PFM_ENTRY_B0[2:0] = 100		175		
		PFM_ENTRY_B0[2:0] = 101		225		
		PFM_ENTRY_B0[2:0] = 110		275		
		PFM_ENTRY_B0[2:0] = 111		325		
I_{ADD}	Phase adding level	ADD_PH_B0[2:0] = 001		400		
		ADD_PH_B0[2:0] = 010		500		mA
		ADD_PH_B0[2:0] = 011		600		
		ADD_PH_B0[2:0] = 100		700		
		ADD_PH_B0[2:0] = 101		800		
		ADD_PH_B0[2:0] = 110		900		
		ADD_PH_B0[2:0] = 111		1000		

(1) Junction-to-ambient thermal resistance value given is valid for High-K PCB, and is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(2) Specifications listed in this table are for 6-phase configuration only. Besides the default 6-phase, single-output voltage rail configuration, the 6 switcher cores can be bundled to a variety of different grouping configurations. For applications requiring other DC-DC converter configuration(s), please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) In the real application, achievable output voltage ramp profiles are influenced by a number of factors, including the amount of output capacitance, the load current level, the load characteristic (either resistive or constant-current), and the voltage ramp amplitude. Typical values are measured with typical conditions. The falling edge ramp rate can be limited by the negative current limit I_{LIMITN}.
(4) The final PFM-to-PWM and PWM-to-PFM switchover current varies slightly and is dependant on the output voltage, input voltage, and the inductor current level. Typical values are measured with typical conditions.

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6-Phase Buck System Characteristics (continued)

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range –40°C ≤ T_A ≤ 85°C; typical (TYP) values at T_A = 25°C (unless otherwise noted)(1)(2). V_{VDDA5V} = V_{VINBXX} = 3.7 V, V_{VIOSYS} = V_{NRST} = 1.8 V, V_{OUT} = 1.1 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SHED}	Phase shedding level	SHED_PH_B0[2:0] = 000		300		mA
		SHED_PH_B0[2:0] = 001		400		
		SHED_PH_B0[2:0] = 010		500		
		SHED_PH_B0[2:0] = 011		600		
		SHED_PH_B0[2:0] = 100		700		
		SHED_PH_B0[2:0] = 101		800		
		SHED_PH_B0[2:0] = 110		900		
ΔV_{OUT}	Line regulation	2.5 V ≤ V_{VINBXX} ≤ 5 V I_{LOAD} = 1 A, forced PWM		0.05		%/V
	Load regulation in PWM mode of operation	100 mA ≤ I_{LOAD} ≤ 10 A, Differential sensing enabled		0.2		%/A
	Transient load step response	AUTO (no Low-Power PFM) mode, I_{OUT} 0.5 mA → 500 mA → 0.5 mA, 100 ns load step		±30		mV
		PWM mode, I_{OUT} 0.6 A → 2 A → 0.6 A, 400-ns load step		±20		mV
		PWM mode, I_{OUT} 1 A → 8 A → 1 A, 400-ns load step		±60		mV
	Transient line response	V_{VINBXX} stepping 3.3 V <—> 3.8 V, t_r = t_f = 10 µs, I_{OUT} = 2000 mA DC		±15		mV
I_{OUT}	Output current	DC load each phase			2500	mA
		Six phases combined(5)			15000	
C_{OUT}	Output capacitance(6)	Effective capacitance during operation, V_{OUT} = 0.6 V to 1.67 V, Min value over T_A –40°C to 85°C	30	50		µF
C_{IN}	Input capacitance on each input voltage rail(6)(7)	Effective capacitance during operation, 2.5 V ≤ V_{VINBXX} ≤ 5 V	2.5	10		µF
L	Output inductance	Effective inductance during operation	0.25	0.47	1	µH
$I_{BALANCE}$	Current balancing accuracy	I_{OUT} ≥ 1000 mA		< 10%		
V_{RIPPLE_PWM}	Output voltage ripple PWM mode, One phase active(8)	C_{OUT} ESR = 10 mΩ PWM mode, I_{OUT} = 200 mA Switching frequency = 4 MHz		7		mV_{PP}
V_{RIPPLE_PFM}	Output voltage ripple PFM mode(8)	C_{OUT} ESR = 10 mΩ PFM mode I_{OUT} = 100 µA		8		mV_{PP}

(5) The power switches in the LP8755 are designed to operate continuously with currents up to the switch current limit thresholds. However, when continuously operating at high current levels there will be significant heat generated within the IC and thus sustained total DC current which the device can support is typically limited by thermal constraints. Thermal issues will become extremely important when designing PCB and the thermal environment of the LP8755. PCB with high thermal efficiency is required to ensure the junction temperature is kept below 125°C. Completing thermal analyses in early stages of the product design process is highly recommended to predict thermal performance at board level. Under high current load conditions the serial bus master device must monitor the temperature of the converter using the Thermal warning feature, see *Protection Features Characteristics*. If the 2nd thermal warning is triggered at 120°C, the application must quickly decrease the load current to keep the converter within its recommended operating temperature.
(6) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics. The performance of the LP8755 device depends greatly on the care taken in designing the Printed Circuit Board (PCB). The use of low inductance and low serial resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the IC and between the power and ground pins to support high peak currents being drawn from System Power Rail during turn-on of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance and capacitance can easily become the performance limiting items.
(7) In addition to these capacitors, at least one higher value capacitor (for example, 22 µF) should be placed close to the power pins. Note that cores B0-B1 and B3-B4 do have combined power input pins.
(8) Ripple voltage should be measured at C_{OUT} electrode on a well-designed PCB, using suggested inductors and capacitors and with a high-quality scope probe.

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6-Phase Buck System Characteristics (continued)

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range –40°C ≤ T_A ≤ 85°C; typical (TYP) values at T_A = 25°C (unless otherwise noted)(1)(2). V_{VDDA5V} = V_{VINBXX} = 3.7 V, V_{VIOSYS} = V_{NRST} = 1.8 V, V_{OUT} = 1.1 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RIPPLE_LP}	Output Voltage Ripple Low-Power PFM mode(8)	C_{OUT} ESR = 10 mΩ Low-power PFM mode I_{OUT} = 100 µA		8		mV_{PP}

6.8 Protection Features Characteristics

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range –40°C ≤ T_A ≤ 85°C; typical (TYP) at T_A = 25°C (unless otherwise noted)(1)(2). V_{VDDA5V} = V_{VINBXX} = 3.7 V, V_{VIOSYS} = V_{NRST} = 1.8 V, V_{OUT} = 1.1 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE MONITORING						
V_{PG}	Power good threshold voltage	Power good threshold for voltage decreasing, % of setting, V_{OUT} = 1.1 V		90%		
V_{OVP}	Input overvoltage protection trigger point(3)(4)	V_{IN} rising. Voltage monitored on VDDA5V pin	5.15	5.3	5.45	V
V_{UVLO}	Input undervoltage lockout (UVLO) turn-on threshold(3)	V_{IN} falling. Voltage monitored on VDDA5V pin	2.15	2.25	2.35	V
V_{SCP}	Output short-circuit fault threshold	Detected by sensing the voltage on converter output with respect to GND.		400		mV
$t_{MASKSCP}$	SCP masking time	Triggered by converter start-up, specified by design		400		µs
t_{MASKPG}	Power Good masking time	Triggered by converter start-up, specified by design		400		µs
		Triggered by VSET transition, specified by design Slew Rate setting mV/µs				
		30		50		µs
		15		100		
		7.5		200		
		3.8		400		
		1.9		800		
		0.94		1600		
		0.47		3200		
		0.23		6400		

(1) Junction-to-ambient thermal resistance value given is valid for High-K PCB, and is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(2) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics. The performance of the LP8755 device depends greatly on the care taken in designing the Printed Circuit Board (PCB). The use of low inductance and low serial resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the IC and between the power and ground pins to support high peak currents being drawn from System Power Rail during turn-on of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance and capacitance can easily become the performance limiting items.
(3) Undervoltage lockout (UVLO) and overvoltage protection (OVP) circuits shut down the LP8755 when the system input voltage is outside the desired operating range.
(4) Limits for OVP trigger points apply when V_{VIOSYS} is high. False OVP alarm may occur, if the input voltage rises close to 5 V while V_{VIOSYS} is low.

Protection Features Characteristics (continued)

Minimum (MIN) and maximum (MAX) limits apply over the full ambient temperature range –40°C ≤ T_A ≤ 85°C; typical (TYP) at T_A = 25°C (unless otherwise noted)(1)(2). V_{VDDA5V} = V_{VINBXX} = 3.7 V, V_{VIOSYS} = V_{NRST} = 1.8 V, V_{OUT} = 1.1 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN AND MONITORING						
T_{SHUT}	Thermal shutdown (TSD)	Threshold, Temperature rising		150		°C
		Hysteresis		25		
T_{WARN}	Thermal warning	Temperature rising, 1st warning, Interrupt only		85		
		Hysteresis		10		
	Thermal warning prior to TSD	Temperature rising, 2nd warning, Interrupt and flag set		120		
		Hysteresis		10		

6.9 I²C Serial Bus Timing Parameters

Serial bus address is selected by the ADDR pin. Connect the pin to GND (addr = 60h), VIOSYS (addr = 61h), SDASYS (addr = 62h), or SCLSYS (addr = 63h). Both of the serial buses share the same address; that is, if addr = 60h is selected for the System bus, the Dynamic Voltage Scaling bus will respond to the same address. Start conditions are used to secure the I²C slave address. During the I²C bus start condition, it is detected whether the ADDR is connected to SDASYS, SCLSYS, GND, or VIOSYS. The I²C host should allow at least 500 µs before sending data to the LP8755 after the rising edge of the VIOSYS line.

These specifications are ensured by design. Limits apply over the full ambient temperature range –40°C ≤ T_A ≤ 85°C, V_{VDDA5V} = V_{VINBXX} = 3.7 V, V_{VIOSYS} = V_{NRST} = 1.8 V, V_{OUT} = 1.1 V (unless otherwise noted) (See Figure 1) .

			MIN	NOM	MAX	UNIT
DIGITAL TIMING SPECIFICATIONS (SCL, SDA)(1)(2)(3)						
f_{CLK}	Serial clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
		High-speed mode, C_b = 100 pF (max)			3.4	MHz
		High-speed mode, C_b = 400 pF (max)(4)			1.7	MHz
t_{LOW}	SCL low time	Standard mode	4.7			µs
		Fast mode	1.3			
		High-speed mode, C_b = 100 pF (max)	160			ns
		High-speed mode, C_b = 400 pF (max)(4)	320			
t_{HIGH}	SCL high time	Standard mode	4			µs
		Fast mode	0.6			
		High-speed mode, C_b = 100 pF (max)	60			ns
		High-speed mode, C_b = 400 pF (max)(4)	120			
$t_{SU;DAT}$	Data setup time	Standard mode	250			ns
		Fast mode	100			
		High-speed mode	10			
$t_{HD;DAT}$	Data hold time	Standard mode	0		3.45	µs
		Fast mode	0		0.9	
		High-speed mode, C_b = 100 pF (max)	0		70	ns
		High-speed mode, C_b = 400 pF (max)(4)	0		150	

(1) Unless otherwise stated, 'SDA' in this paragraph refers to both of the SDASR and SDASYS signals, and respectively 'SCL' refers to SCLSR and SCLSYS signals.
(2) C_b refers to the capacitance of one bus line. C_b is expressed in pF units. The specification table provided applies to both of the interfaces; DVS and System interface.
(3) The power-on default setting for the system bus and the DVS bus is High-speed-enabled, there is no handshaking required to initiate high speed.
(4) For bus line loads C_b between 100 pF and 400 pF the timing parameters must be linearly interpolated.

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I²C Serial Bus Timing Parameters (continued)

Serial bus address is selected by the ADDR pin. Connect the pin to GND (addr = 60h), VIOSYS (addr = 61h), SDASYS (addr = 62h), or SCLSYS (addr = 63h). Both of the serial buses share the same address; that is, if addr = 60h is selected for the System bus, the Dynamic Voltage Scaling bus will respond to the same address. Start conditions are used to secure the I²C slave address. During the I²C bus start condition, it is detected whether the ADDR is connected to SDASYS, SCLSYS, GND, or VIOSYS. The I²C host should allow at least 500 µs before sending data to the LP8755 after the rising edge of the VIOSYS line.

These specifications are ensured by design. Limits apply over the full ambient temperature range –40°C ≤ T_A ≤ 85°C, V_{VDDA5V} = V_{VINBXX} = 3.7 V, V_{VIOSYS} = V_{NRST} = 1.8 V, V_{OUT} = 1.1 V (unless otherwise noted) (See Figure 1) .

			MIN	NOM	MAX	UNIT
$t_{SU;STA}$	Set-up time for a repeated start condition	Standard mode	4.7			µs
		Fast mode	0.6			µs
		High-speed mode	160			ns
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard mode	4.0			µs
		Fast mode	0.6			µs
		High-speed mode	160			ns
t_{BUF}	Bus free time between a stop and start condition	Standard mode	4.7			µs
		Fast mode	1.3			µs
$t_{SU;STO}$	Set-up time for a stop condition	Standard mode	4.0			µs
		Fast mode	0.6			µs
		High-speed mode	160			ns
t_{rDA}	Rise time of SDA signal	Standard mode			1000	ns
		Fast mode	20		300	ns
		High-speed mode, C_b = 100 pF (max)	10		80	ns
		High-speed mode, C_b = 400 pF (max)(4)	20		160	ns
t_{fDA}	Fall time of SDA signal	Standard mode			300	ns
		Fast Mode	6.5		300	ns
		High-speed mode, C_b = 100 pF (max)	10		80	ns
		High-speed mode, C_b = 400 pF (max)(4)	20		160	ns
t_{rCL}	Rise time of SCL signal	Standard mode			1000	ns
		Fast mode	20		300	ns
		High-speed mode, C_b = 100 pF (max)	10		40	ns
		High-speed mode, C_b = 400 pF (max)(4)	20		80	ns
t_{rCL1}	Rise time of SCL signal after a repeated start condition and after acknowledge bit	High-speed mode, C_b = 100 pF (max)	10		80	ns
		High-speed mode, C_b = 400 pF (max)(4)	20		160	ns
t_{fCL}	Fall time of a SCL signal	Standard mode			300	ns
		Fast mode	6.5		300	ns
		High-speed mode, C_b = 100 pF (max)	10		40	ns
		High-speed mode, C_b = 400 pF (max)(4)	20		80	ns
C_b	Capacitive load for each bus line (SCL and SDA)				400	pF
t_{SP}	Pulse width of spike suppressed(5)	Fast mode			50	ns
		High-speed mode			10	ns

(5) Spike suppression filtering on SCLSYS, SCLSR, SDASYS and SDASR will suppress spikes that are less than the indicated width.

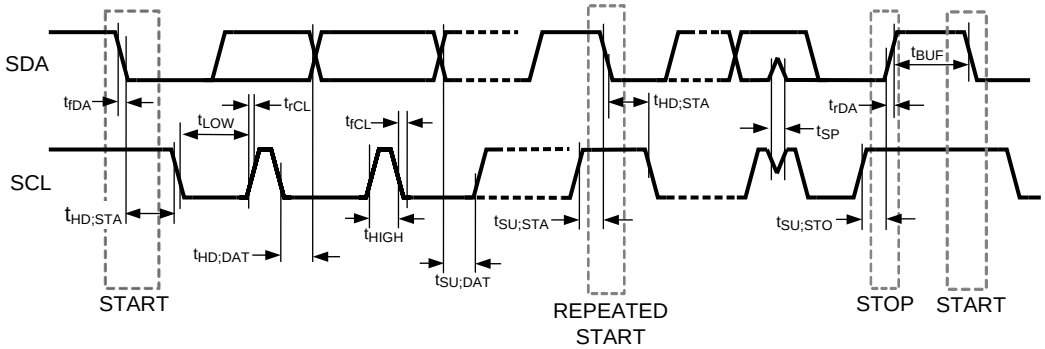

Figure 1. I²C Timing

6.10 Typical Characteristics

Unless otherwise specified: V_{VDDA5V} = V_{VINBXX} = 3.7 V

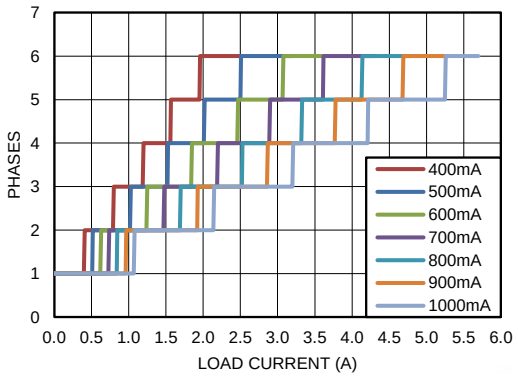

Figure 2. Phase Adding vs Load Current in Different ADD_PH_B0 Settings

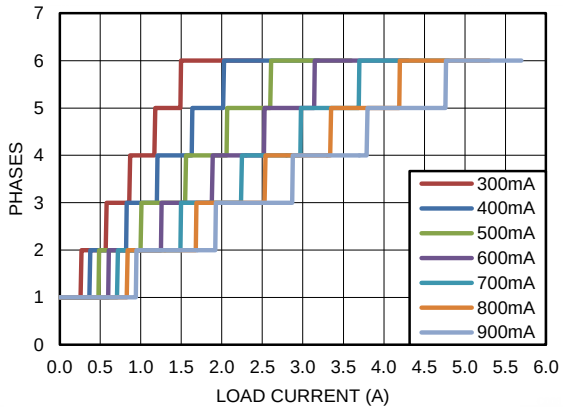

Figure 3. Phase Shedding vs Load Current in Different SHED_PH_B0 Settings

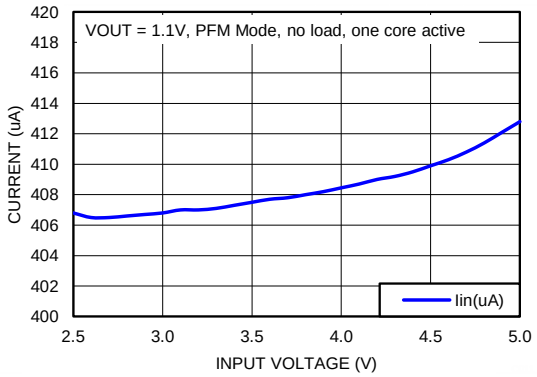

Figure 4. PFM Mode Current Consumption vs V_{IN}

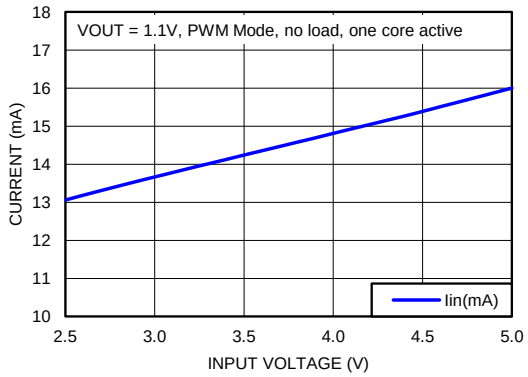

Figure 5. PWM Mode Current Consumption vs V_{IN}

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7 Detailed Description

7.1 Overview

The LP8755 is a high-efficiency, high-performance power supply IC with six step-down DC-DC converter cores. It delivers 0.6 V to 1.67 V regulated voltage rail from either a single Li-Ion or three cell NiMH/NiCd batteries to portable devices such as cell phones and PDAs.

There are three modes of operation for the 6-phase converter, depending on the output current required: PWM (Pulse Width Modulation), PFM (Pulse-Frequency Modulation), and Low-Power PFM. Converter operates in PWM mode at high load currents of approximately 250 mA or higher, depending on register setting. Lighter output current loads will cause the converter to automatically switch into PFM or Low-Power PFM mode for reduced current consumption and a longer battery life. Forced PWM is also available for highest transient performance.

Under no-load conditions the device can be set to Standby or Shutdown. Shutdown mode turns off the device, offering the lowest current consumption (I_{SHDN} = 0.1 µA typ.). Additional features include soft-start, undervoltage lockout, input overvoltage protection, current overload protection, thermal warning, and thermal shutdown.

The modes and features can be programmed via control registers. All the registers can be accessed with both I^2C serial interfaces: System serial interface and Dynamic voltage scaling (DVS) interface. Using DVS interface for dynamic voltage scaling prevents latencies if System serial interface is busy. Using DVS interface is optional; System serial interface can also be used for dynamic voltage scaling.

7.1.1 Buck Information

The LP8755 has six integrated high-efficiency buck converter cores. The cores are designed for flexibility; most of the functions are programmable, thus allowing optimization of the SMPS operation for each application. The cores are bundled together to establish a multi-phase converter This is shown in Figure 23.

Operating Modes:

- OFF: Output is isolated from the input voltage rail in this mode. Output has an optional pulldown resistor.
- PWM: Converter operates in buck configuration. Average switching frequency is constant.
- PFM: Converter switches only when output voltage decreases below programmed threshold. Inductor current is discontinuous.
- Low-Power PFM: This mode is similar to PFM mode, but used with lower load conditions. In this mode some of the internal blocks are turned off between the PFM pulses. Load transient response is compromised due to the wake-up time.

Features:

- DVS support; SmartReflex functionality
- Automatic mode control based on the loading
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Power good flag with maskable interrupt
- Overvoltage comparator
- Phase control and spread spectrum techniques for reducing EMI
- Average output current sensing (for PFM/PWM entry/exit, phase adding/shedding, and load current reporting)
- Current balancing between the phases of the converter
- Differential voltage sensing
- Dynamic phase adding/shedding, each output being phase shifted

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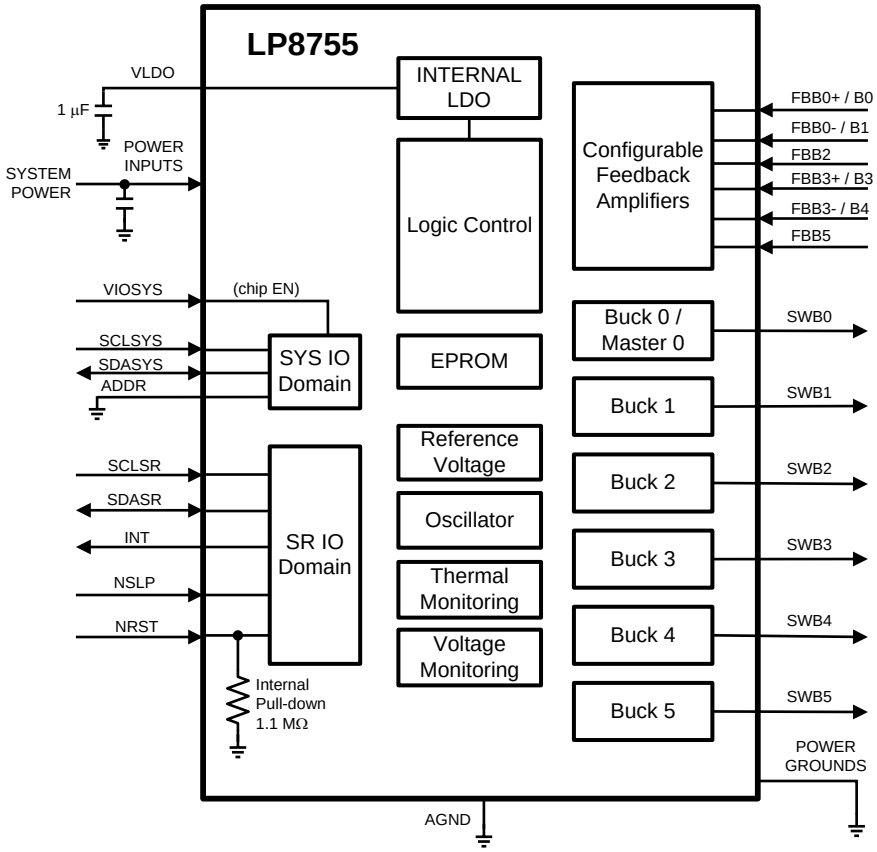
Overview (continued)

Programmability (The following parameters can be programmed via registers):

- Output voltage
- Forced PWM operation
- Switch current limits for high side FET
- PWM/PFM mode entry and exit (based on average output current)
- Phase adding and shedding levels
- Output voltage slew rate

7.2 Functional Block Diagram



7.3 Features Descriptions

7.3.1 Multi-Phase DC-DC Converters

A multi-phase synchronous buck converter offers several advantages over a single power-stage converter. For application processor power delivery, lower ripple on the input and output currents and faster transient response to load steps are the most significant advantages. Also, since the load current is evenly shared among multiple channels, the heat generated is greatly reduced for each channel due to the fact that power loss is proportional to square of current. Physical size of the output inductor shrinks significantly for the similar reason. Interleaving switching action of the converters and channels for a typical application (shown in Figure 23) is illustrated in Figure 7.

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Features Descriptions (continued)

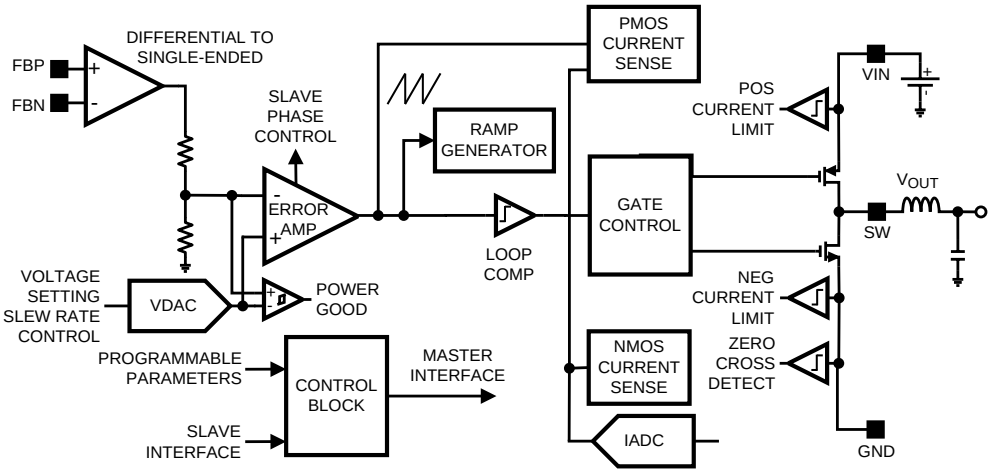

Figure 6. Detailed Block Diagram Showing One Buck Core

7.3.1.1 Multi-Phase Operation and Phase-Shedding

Under heavy load conditions, the 6-phase converter switches each channel 60° apart. As a result, the 6-phase converter has an effective ripple frequency six times greater than the switching frequency of any one phase. However, the parallel operation decreases the efficiency at light load conditions. In order to overcome this operational inefficiency, the LP8755 changes the number of active phases to optimize efficiency for the variations of the load. This is called phase-shedding. The concept is illustrated in Figure 7.

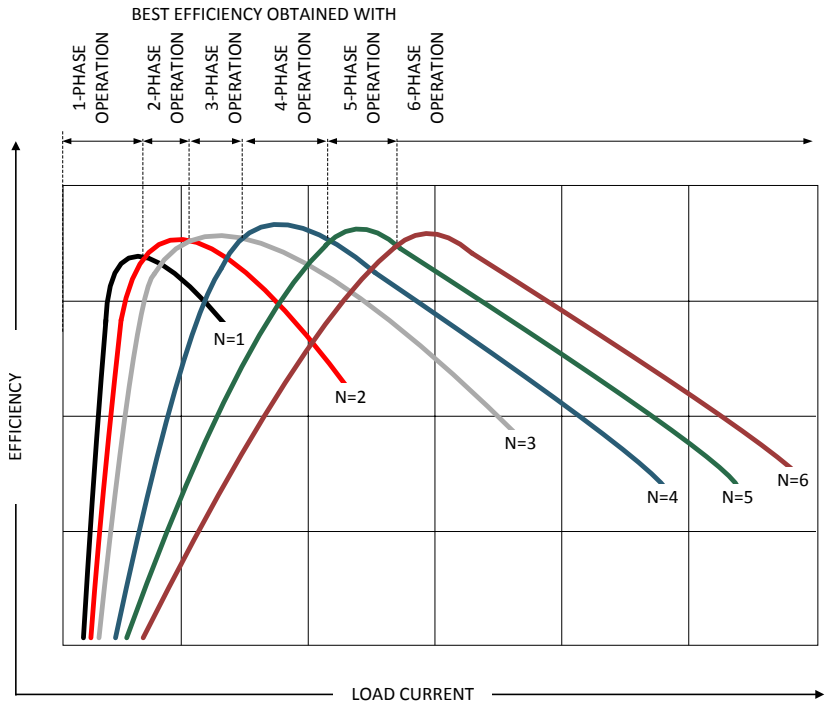

Figure 7. Multi-phase Buck Converter Efficiency vs Number of Phases; All Converters in PWM Mode (6)

(6) Graph is not to scale and is for illustrative purposes only.

Features Descriptions (continued)

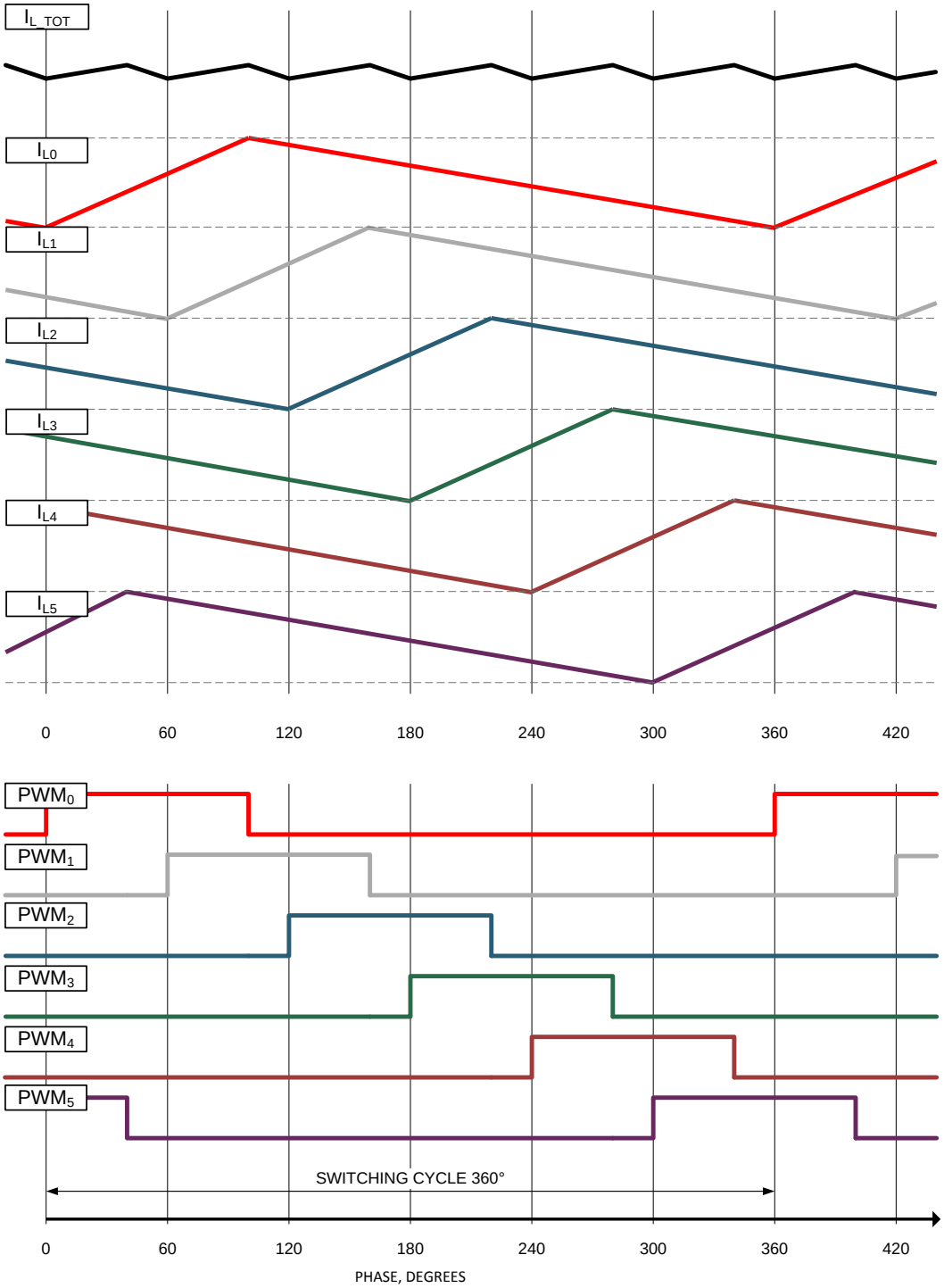

Figure 8. PWM Timings and Inductor Current Waveforms (7)

(7) Graph is not to scale and is for illustrative purposes only.

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Features Descriptions (continued)

7.3.1.2 Transitions Between Low-Power PFM, PFM, and PWM Modes

Normal PWM-mode operation with phase-shedding can optimize efficiency at mid-to-full load, but this is usually at the expense of light-load efficiency. The LP8755 converter operates in PWM mode at a load current of 100 to 375 mA or higher; this mode transition trip-point is set by register. Lighter load current causes the device to automatically switch into PFM mode for reduced current consumption. By combining PFM and PWM modes in the same regulator and providing automatic switching, high efficiency can be achieved over a wide output load current range.

Efficiency is further enhanced when the converter enters Low-Power PFM mode. The LP8755 includes Low-Power mode function for low-current consumption. In this mode most of the internal blocks are disabled between the inductor current ramp up and ramp down phases to reduce the operating current. However, as a result, the transient performance of the converter is compromised. The Low-Power mode can be enabled by control register setting. Also, the application processor or the PMIC may provide an HW signal (NSLP) to the LP8755 input to indicate when the processor has entered a low-power state. When the signal is asserted, the LP8755 Low-Power PFM function will be enabled, and the LP8755 will run with a reduced input current. The right timing of the NSLP signal from the system is important for best load-transient performance. The NSLP signal should be asserted only when load current is stable and below 30 mA. Before the load current increases above 30 mA, the NSLP signal should be de-asserted 100 µs (minimum) prior to a load step to prepare the converter for the higher load current.

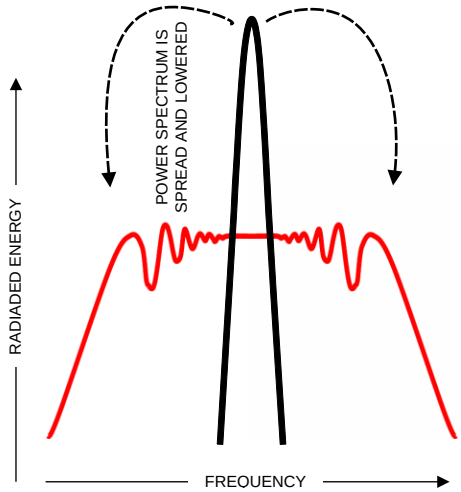
7.3.1.3 Buck Converter Load Current

The buck load current can be monitored via I^2C registers. Current of different buck converter cores or the total load current of the master can be selected from register 0x21 (see *SEL_I_LOAD*). A write to this selection register starts a current measurement sequence. The measurement sequence is a minimum of 50 µs long. When a measurement sequence starts, the FLAGS_1.I_LOAD_READY bit in register 0x0E is set to '0'. After the measurement sequence is finished, the FLAGS_1.I_LOAD_READY bit is set to '1'. (Note that by default this bit is '0'.) The measurement result can be read from registers 0x22 (LOAD_CURR.BUCK_LOAD_CURR[7:0]) and 0x21 (SEL_I_LOAD.BUCK_LOAD_CURR[10:8]). The measurement result [10:0] LSB is 10 mA, and the maximum value of the measurement is 20 A. The LP8755 can be configured to give out an interrupt after the load current measurement sequence is finished. Load current measurement interrupt can be masked with INT_MASKS_2.MASK_I_LOAD_READY bit.

7.3.1.4 Spread Spectrum Mode

Systems with periodic switching signals may generate a large amount of switching noise in a set of narrowband frequencies (the switching frequency and its harmonics). The usual solution to reduce noise coupling is to add EMI-filters and shields to the boards. The LP8755's register-selectable spread spectrum mode minimizes the need for output filters, ferrite beads, or chokes. In spread spectrum mode, the switching frequency varies randomly around the center frequency, reducing the EMI emissions radiated by the converter, associated passive components, and PCB traces. See Figure 9.

Features Descriptions (continued)



Where a fixed-frequency converter exhibits large amounts of spectral energy at the switching frequency, the spread spectrum architecture of the LP8755 spreads that energy over a large bandwidth.

Figure 9. Spread Spectrum Modulation

7.3.2 Power-Up and Output Voltage Sequencing

The power-up sequence for the LP8755 is as follows:

- V_{VINBXX} and V_{VDDA5V} reach min recommended levels.
- V_{VIOSYS} set high. Enables the system I/O interface. For power-on-reset (POR), the I^2C host should allow at least 500 µs before sending data to the LP8755 after the rising edge of the VIOSYS line.
- V_{LDO} voltage is raising. The LDO voltage is generated internally. The internal POR signal is activated.
- Internal POR deasserted, OTP read.
- Device enters standby mode.
- DC-DC enable, output voltage, voltage slew rate programmed over I^2C as needed by the application.
- NRST set high.

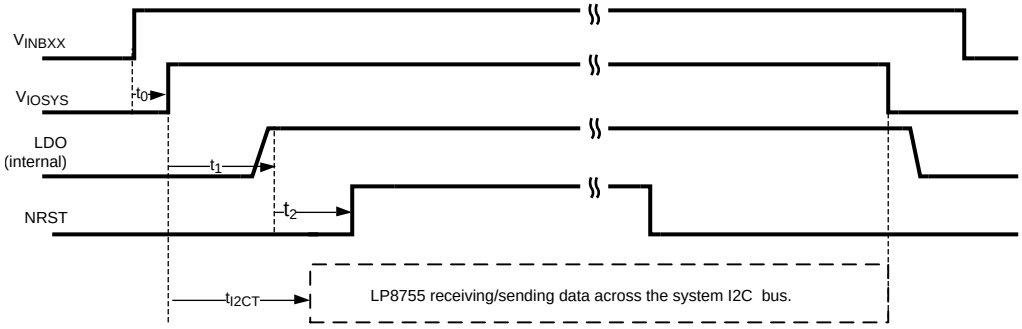


Figure 10. Timing Diagram for the Power-Up Sequence

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Features Descriptions (continued)

Table 1. Power-Up Sequence

PARAMETER		CONDITION (1)	MIN	TYP	MAX	UNIT
t_0	V_{VDDA5V} to V_{VIOSYS} assertion		0			µs
t_1	LDO_{ON} Delay Time	C_{LDO} = 1 µF		<100	150	µs
t_2	LDO_{ON} to NRST HIGH		0			µs
t_{I2CT}	Device ready for I^2C data transfer		500			µs

(1) These specification table entries are specified by design. The power input lines V_{VINBXX}, V_{VDDA5V} and V_{VIOSYS} must be stable before the NRST line goes High. Also, the V_{LDO} line must be stable 1.8 V before the NRST line goes High.

7.3.3 Device Reset Scenarios

There are three reset methods implemented on the LP8755:

- Software reset
- Hardware reset
- Power-on reset (POR)

An SW-reset occurs when the RESET.SW_RESET bit is written first with 1, followed by 0 right after that. This event resets the control registers shown in Table 2 to the default values. The temperature, power good, and other faults are persistent over the SW reset to allow for the system to identify to cause of the failure.

An internal power-on reset (POR) occurs when the supply voltage (V_{VDDA5V}) transitions above the POR threshold or V_{VIOSYS} is toggled low/high. Each of the registers contain a factory-defined value upon POR, and this data remains there until any of the following occurs:

- Device sets a Flag bit, causing the Status register to be updated. The other registers remain untouched.
- A different data word is written to a writable register.

The internal registers will lose their contents if the supply voltage (V_{VDDA5V}) goes below 1 V (typ.).

An NRST high-to-low transition initiates the hardware reset. This event resets the control registers shown in Table 2 to the default values.

Under OVP, UVLO, TSD, or V_{VIOSYS} low (while NRST still high) conditions, a Fast Power-Down is launched.

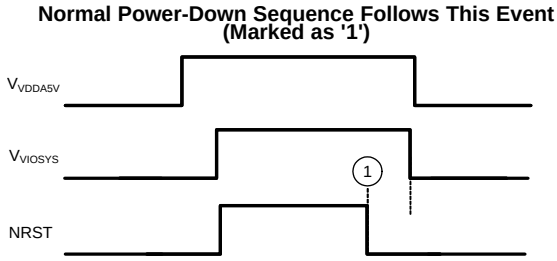

Figure 11. The External Power Control System De-asserts NRST

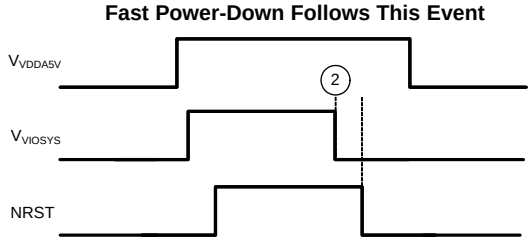

Figure 12. NRST Stays HIGH While V_{VIOSYS} Transition from HIGH to LOW Happens (Marked as '2')

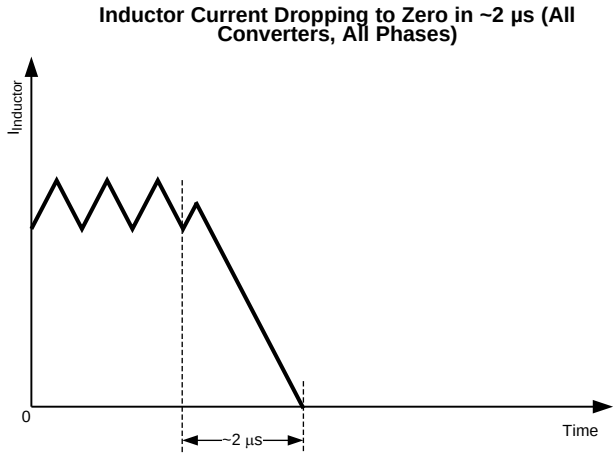

Figure 13. Fast Power-Down

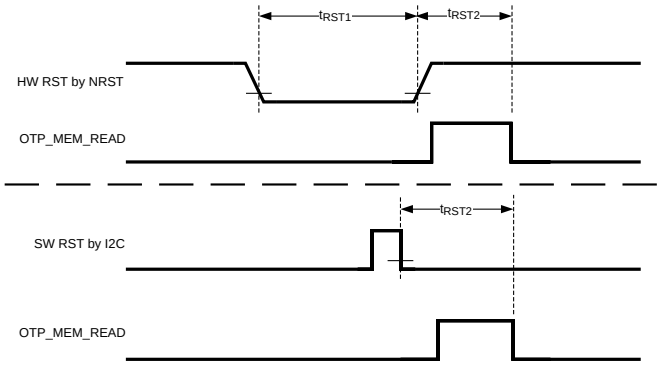

Figure 14. Reset Timings

PARAMETER		LIMIT
t_{RST1}	NRST active low pulse width	1 µs min + value on DELAY register.
t_{RST2}	NRST inactive or I^2C reset event to MEMORY READ end	25 µs max

Table 2. Hardware Reset, Power-On Reset (POR) and Software Reset: Registers After Reset

HEX ADDRESS	REGISTER	SOFTWARE RESET I^2C RESET	HARDWARE RESET NRST LOW (1)	POWER-ON RESET V_{VIOSYS} LOW
0x00	VSET_B0	All bits retained	All bits retained	All bits cleared
0x06	FPWM	All bits cleared	All bits cleared	All bits cleared
0x07	BUCK0_CTRL	All bits cleared	All bits cleared	All bits cleared
0x0D	FLAGS_0	All bits retained	All bits retained	All bits cleared
0x0E	FLAGS_1	All bits retained	All bits retained	All bits cleared
0x0F	INT_MASK0	All bits cleared	All bits cleared	All bits cleared
0x10	GENERAL	All bits cleared	All bits cleared	All bits cleared
0x11	RESET	N/A	All bits cleared	All bits cleared
0x12	DELAY_BUCK0	All bits cleared	All bits cleared	All bits cleared
0x18	CHIP_ID	Read Only		
0x19	PFM_LEV_B0	All bits cleared	All bits cleared	All bits cleared
0x1F	PHASE_LEV_B0	All bits cleared	All bits cleared	All bits cleared
0x21	SEL_I_LOAD	All bits retained	All bits retained	All bits cleared
0x22	LOAD_CURR	Read Only		
0x2E	INT_MASK_2	All bits cleared	All bits cleared	All bits cleared

(1) Reset is falling-edge sensitive and it will take effect upon complete of the power-down sequence. The registers can be updated by I2C writing when NRST is low.

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7.3.4 Diagnosis and Protection Features

The LP8755 is capable of providing two levels of protection features: warnings for diagnosis and faults which are causing the converters to shut down. When the device detects warning or fault conditions, the LP8755 sets the flag bits indicating which fault or warning conditions have occurred; the INT pin will be pulled low. INT will be released again after a clear of flags is complete. The flag bits are persistent over reset to allow for the system to identify what was causing the interrupt and/or converter shutdown.

Also, the LP8755 has a soft-start circuit that limits in-rush current during start-up. The output voltage increase rate is 30 mV/µs (default) during soft-start.

Table 3. Summary of Exceptions and Interrupt Signals

EVENT	REGISTER.BIT	INTERRUPT SIGNAL PRODUCED?	INT MASK AVAILABLE?
SCP triggered	FLAGS_1.SCP	Yes	Yes
Not PowerGood	FLAGS_0.nPG	Yes	Yes
TEMP status change	FLAGS_0.TEMP[1:0]	On any temperature change except for the case when TEMP[1:0] = 0b11	Yes
Thermal warning	FLAGS_1.T_WARNING	Yes	Yes
Thermal shutdown	FLAGS_1.THSD	Yes	No
OVP triggered	FLAGS_1.OVP	Yes	Yes
Load current measurement ready	FLAGS_1.I_LOAD_READY	Yes	Yes
UVLO triggered	FLAGS_1.UVLO	Yes	Yes

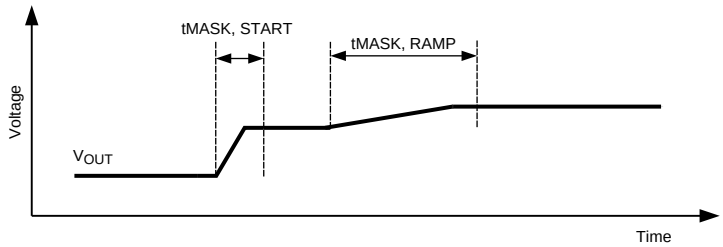
7.3.4.1 Warnings for Diagnosis (No Power Down)

7.3.4.1.1 Short-Circuit Protection (SCP)

A short-circuit protection feature allows the LP8755 to protect itself and external components during overload conditions. The output short-circuit fault threshold is 400 mV (typ.) .

7.3.4.1.2 Power Good Monitoring

When the converter's feedback-pin voltage falls lower than 90% (typ.) of the set voltage, the FLAGS_0.nPG flag is set. To prevent a false alarm, the power good circuit is masked during converter start-up and voltage transitions. The duration of the power good mask is set to 400 µs for converter start-up. For voltage ramps the masking time is extended by an internal logic circuit up to 6.4 ms. (See *Protection Features Characteristics*.)



Masking time for start-up is constant 400 µs (typ.). Masking time for voltage transitions depends on the selected ramp rates.

Figure 15. Power Good Masking Principle

7.3.4.1.3 Thermal Warnings

Prior to the thermal shutdown, thermal warnings are set. The first warning is set at 85°C (INT pin low), and the second at 120°C (INT pin pulled low and FLAGS_1.T_WARNING flag set). If the chip temperature crosses any of the thresholds of 85°C, 120°C, or 150°C (see *FLAGS_0* register) the INT pin will be triggered. INT will be cleared upon read of FLAGS_0.TEMP[1:0] bits except if FLAGS_0.TEMP [1:0] = 0b11, which is a thermal fault event.

7.3.4.2 Faults (Fault State and Fast Power Down)

7.3.4.2.1 Undervoltage Lockout (UVLO)

When the input voltage falls below V_{UVLO} (typ. 2.25 V) at the VDDA5V pin, the LP8755 indicates a fault by activating the FLAGS_1.UVLO flag. The buck converter shut down without a power-down sequence(Fast Power-Down). The flag will remain active until the input voltage is raised above the UVLO threshold. If the flag is cleared while the fault persists, the flag is immediately re-asserted, and interrupt remains active.

7.3.4.2.2 Overvoltage Protection (OVP)

When an input voltage greater than V_{OVP} (typ. 5.3 V) is detected at the VDDA5V pin, the LP8755 indicates a fault by activating the FLAGS_1.OVP flag. The buck converter shut down without power-down sequence (Fast Power-Down). The flag will remain active until the input voltage is below the OVP threshold. If the flag is cleared while the fault persists, the flag is immediately re-asserted and interrupt remains active.

7.3.4.2.3 Thermal Shutdown (THSD)

The LP8755 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device enters shutdown via fault-state. INT will be cleared upon write of the FLAGS_1.THSD flag even when thermal shutdown is active. This allows automatic recovery when temperature decreases below thermal shutdown level. See Figure 16 for LP8755 thermal diagnosis and protection features.

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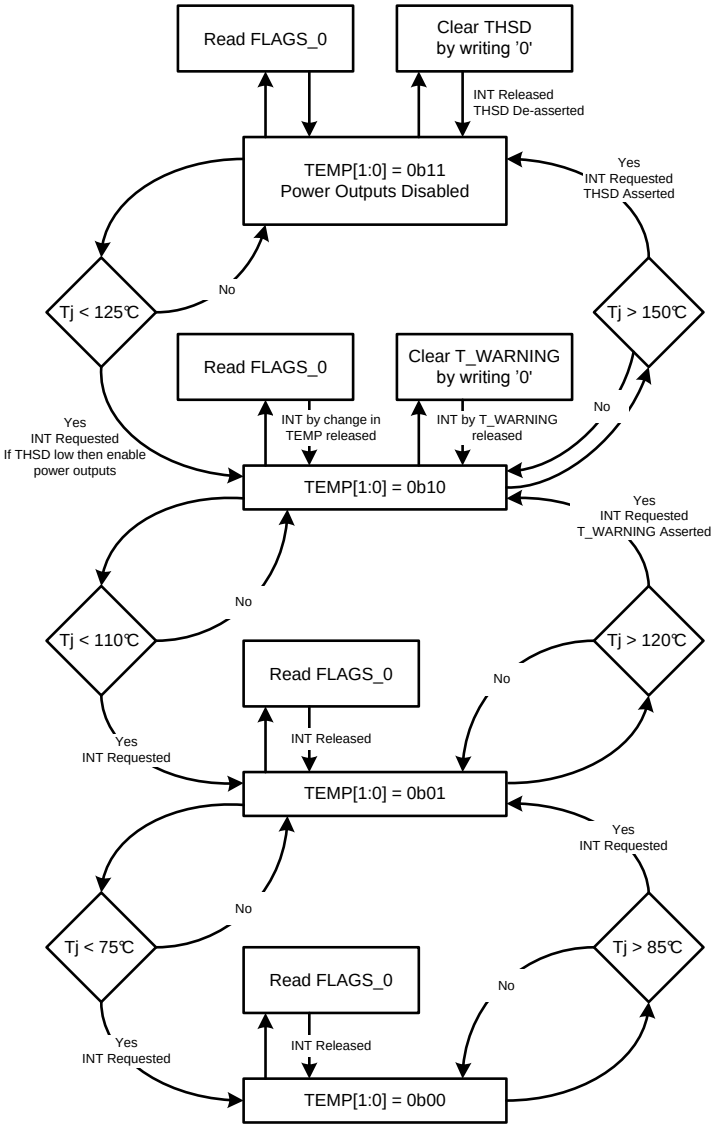

Note that INT is asserted whenever any of the thermal thresholds is crossed, if unmasked. Note also the 10°C Hysteresis on the T_J Thresholds.

Figure 16. Thermal Warnings and Thermal Shutdown Flow

7.4 Device Functional Modes

SHUTDOWN: All switch, reference, control and bias circuitry of the LP8755 are turned off. The main battery supply voltage is high enough to start the buck power-up sequence but V_{VIOSYS} and NRST are LOW.

STANDBY: Setting V_{VIOSYS} HIGH enables standby-operation. All registers can be read or written by the system master via the system serial interface. Recovery from UVLO, TSD, or OVP event also leads to standby.

ACTIVE: Regulated DC-DC converters are on or can be enabled with full current capability. In this mode, all features and control registers are available via the system serial bus and via SmartReflex interface.

LOW-POWER: At light loads (less than approximately 30 mA), and when the load does not require highest level of transient performance, the device enters automatically Low-Power mode. In this mode the part operates at low I_Q. Conditions entering and exiting Low-Power mode are shown in Figure 17.

Device Functional Modes (continued)

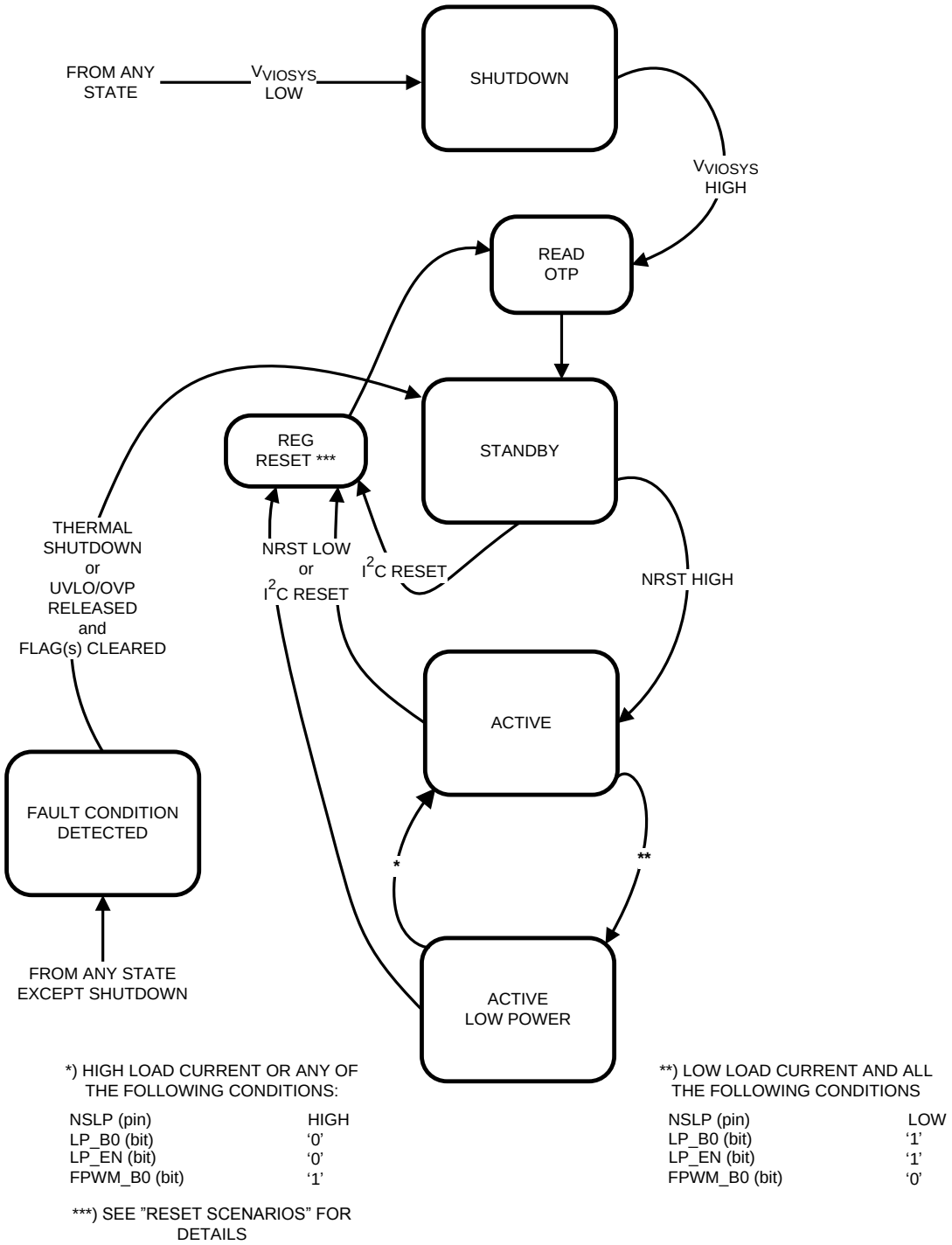

Figure 17. Device Operation Modes

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7.5 Programming

7.5.1 I²C-Compatible Interface

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines should each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle. Note: CLK pin is not used for serial bus data transfer. There are two buses implemented: the System I²C bus and the SmartReflex bus. In the following paragraphs, SCL refers to both SCLSYS and SCLSR, and SDA refers to SDASYS and SDASR. The LP8755 supports standard mode (100 kHz), fast mode (400 kHz) and high-speed mode (3.4 MHz).

7.5.1.1 Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW.

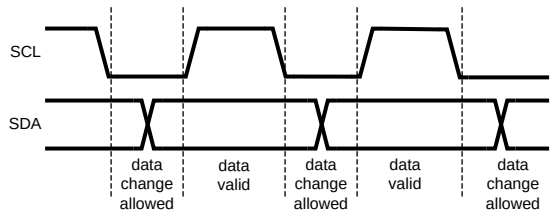


Figure 18. Data Validity Diagram

7.5.1.2 Start and Stop Conditions

The LP8755 is controlled via an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as SDA transitions from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transition from LOW to HIGH while SCL is HIGH. The I²C master always generates the START and STOP conditions.

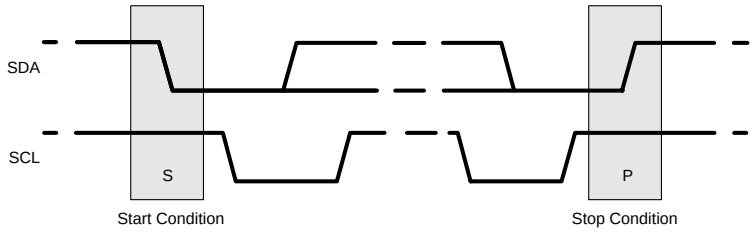


Figure 19. Start and Stop Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I²C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. Figure 1 shows the SDA and SCL signal timing for the I²C-Compatible Bus. See the *I²C Serial Bus Timing Parameters* for timing values.

7.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LP8755 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LP8755 generates an acknowledge after each byte has been received.

Programming (continued)

There is one exception to the “acknowledge after every byte” rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

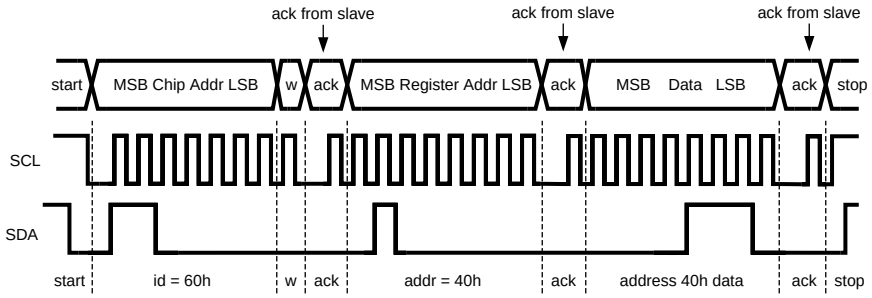
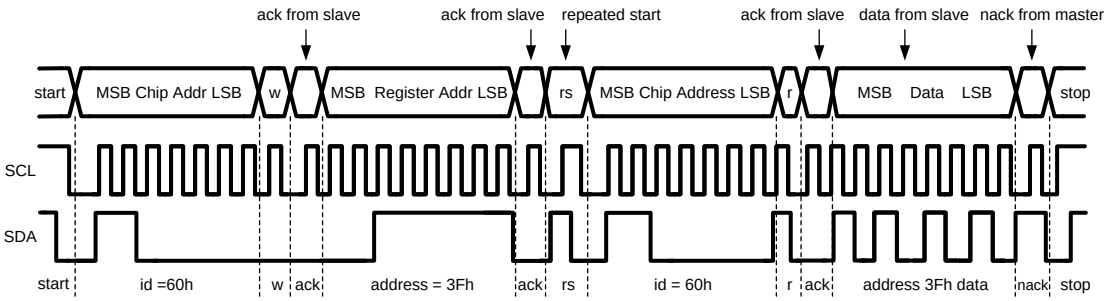


Figure 20. Write Cycle (w = write; SDA = '0'), id = device address = 60Hex for LP8755.

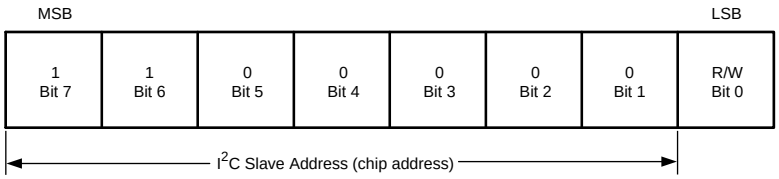


When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

Figure 21. Read Cycle (r = read; SDA = '1'), id = device address = 60Hex for LP8755.

7.5.1.4 I²C-Compatible Chip Address

The device address for the LP8755 is 0x60 (ADDR pin tied to the GND). After the START condition, the I²C master sends the 7-bit address followed by an eighth bit, read or write (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data will be written. The third byte contains the data for the selected register.



Here device address is 1100000Bin = 60 Hex.

Figure 22. Device Address

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Programming (continued)

7.5.1.5 Auto-Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the LP8755, the internal address index counter will be incremented by one, and the next register will be written. Table 4 shows writing sequence to two consecutive registers. Note: the auto-increment feature does not work for read.

Table 4. Auto-Increment Example

Master Action	Start	Device Address = 60H	Write		Register Address		Data		Data		Stop
LP8755 Action				ACK		ACK		ACK		ACK	

7.6 Register Maps

7.6.1 Register Descriptions

The LP8755 is controlled by a set of registers through the system serial interface port or through the SmartReflex-compatible interface. Table 5 lists device registers, their addresses and their abbreviations. A more detailed description is given in the sections *VSET_B0* to *INT_MASK_2*.

Many registers contain bits, that are reserved for future use. When writing to a register, any reserved bits should not be changed.

Table 5. Register Descriptions

Addr	Register	Read / Write	D7	D6	D5	D4	D3	D2	D1	D0
0x00	VSET_B0	R/W	EN_DIS_B0	VSET_B0[6:0]						
0x06	FPWM	R/W	Reserved							FPWM_B0
0x07	BUCK0_CTRL	R/W	OC_LEV_B0[1:0]		LP_B0	RDIS_B0	Reserved	RAMP_B0[2:0]		
0x0D	FLAGS_0	R/W	Reserved					nPG_B0	TEMP[1:0]	
0x0E	FLAGS_1	R/W	Reserved		I_LOAD_READY	UVLO	T_WARNING	THSD	OVP	SCP
0x0F	INT_MASK_0	R/W	Reserved					MASK_nPG_B0	MASK_OVP	MASK_SCP
0x10	GENERAL	R/W	Reserved		EN_SS	Reserved	DIS_DIF_B0	Reserved	SLP_POL	LP_EN
0x11	RESET	R/W	Reserved							SW_RESET
0x12	DELAY_BUCK0	R/W	DELAY_B0[7:0]							
0x18	CHIP_ID	R	VENDOR[1:0]		ALL_LAYER[1:0]		METAL_LAYER[3:0]			
0x19	PFM_LEV_B0	R/W	Reserved	PFM_ENTRY_B0[2:0]			Reserved	PFM_EXIT_B0[2:0]		
0x1F	PHASE_LEV_B0	R/W	Reserved	ADD_PH_B0[2:0]			Reserved	SHED_PH_B0[2:0]		
0x21	SEL_I_LOAD	R/W	Reserved	BUCK_LOAD_CURR[10:8]			Reserved	LOAD_CURRENT_SOURCE[2:0]		
0x22	LOAD_CURR	R	BUCK_LOAD_CURR[7:0]							
0x2E	INT_MASK_2	R/W	Reserved				MASK_ILOAD_READY	MASK_UVLO	MASK_TWARNING	MASK_TEMP

7.6.2 VSET_B0

Address: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
EN_DIS_B0	VSET_B0[6:0]						

Bits	Field	Type	Default	Description
7	EN_DIS_B0	R/W	1	DC-DC converter Buck0 Enable/Disable. The Enable of the master Buck0 controls the operation of the slave bucks. 0 = Converter disabled 1 = Converter enabled Note: When a disable request is received the converter is disabled immediately.
6:0	VSET_B0[6:0]	R/W	011 1100	Sets the output voltage. Defined by: V_{OUT} = 0.5 V + 10 mV * VSET_B0 V_{OUT} range = 0.6 V to 1.67 V NOTE: Do not use VSET_B0 values < 0001010 (10 dec) = 0.6 V. NOTE: Register settings starting from 1110110 up to 1111111 are clamped to 1.67 V.

7.6.3 FPWM

Address: 0x06

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							FPWM_B0

Bits	Field	Type	Default	Description
7:1	Reserved	R/W	001 1111	
0	FPWM_B0	R/W	1	Forced PWM mode of operation, Buck regulator 0 (Master). The setting of the master controls the operation of the slave bucks. 0 = PWM, PFM or Low-Power PFM operation mode. 1 = This will force the master converter and the slaves to operate always in the PWM mode.

7.6.4 BUCK0_CTRL

Address: 0x07

D7	D6	D5	D4	D3	D2	D1	D0
OC_LEV_B0[1:0]		LP_B0	RDIS_B0	Reserved	RAMP_B0[2:0]		

Bits	Field	Type	Default	Description
7:6	OC_LEV_B0[1:0]	R/W	11	Inductor positive current limit on Buck 0. Note that OC_LEV_B0...B5 should have the same value. 00 = 1.5 A 01 = 2.0 A 10 = 2.5 A 11 = 3.0 A
5	LP_B0	R/W	0	Allows converter to enter into Low-Power PFM mode. 1 = Entering to Low-Power PFM mode is allowed. 0 = Entering to Low-Power PFM more is not allowed.
4	RDIS_B0	R/W	1	Enables the output discharge resistors when the V_{OUT} supply has been disabled. 1 = Enable pull-down 0 = Disable pull-down
3	Reserved	R/W	0	

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Bits	Field	Type	Default	Description
2:0	RAMP_B0[2:0]	R/W	001	This set the output voltage change ramp as follows: 000 = 30 mV/µs 001 = 15 mV/µs 010 = 7.5 mV/µs 011 = 3.8 mV/µs 100 = 1.9 mV/µs 101 = 0.94 mV/µs 110 = 0.47 mV/µs 111 = 0.23 mV/µs

7.6.5 BUCK1_CTRL

Address: 0x08

D7	D6	D5	D4	D3	D2	D1	D0
OC_LEV_B1[1:0]		Reserved					

Bits	Field	Type	Default	Description
7:6	OC_LEV_B1[1:0]	R/W	11	Inductor positive current limit on Buck 1. Note that OC_LEV_B0...B5 should have the same value. 00 = 1.5 A 01 = 2.0 A 10 = 2.5 A 11 = 3.0 A
5:0	Reserved	R/W	01 0001	

7.6.6 BUCK2_CTRL

Address: 0x09

D7	D6	D5	D4	D3	D2	D1	D0
OC_LEV_B2[1:0]		Reserved					

Bits	Field	Type	Default	Description
7:6	OC_LEV_B2[1:0]	R/W	11	Inductor positive current limit on Buck 2. Note that OC_LEV_B0...B5 should have the same value. 00 = 1.5 A 01 = 2.0 A 10 = 2.5 A 11 = 3.0 A
5:0	Reserved	R/W	01 0001	

7.6.7 BUCK3_CTRL

Address: 0x0A

D7	D6	D5	D4	D3	D2	D1	D0
OC_LEV_B3[1:0]		Reserved					

Bits	Field	Type	Default	Description
7:6	OC_LEV_B3[1:0]	R/W	11	Inductor positive current limit on Buck 3. Note that OC_LEV_B0...B5 should have the same value. 00 = 1.5 A 01 = 2.0 A 10 = 2.5 A 11 = 3.0 A
5:0	Reserved	R/W	01 0001	

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7.6.8 BUCK4_CTRL

Address: 0x0B

D7	D6	D5	D4	D3	D2	D1	D0
OC_LEV_B4[1:0]		Reserved					

Bits	Field	Type	Default	Description
7:6	OC_LEV_B4[1:0]	R/W	11	Inductor positive current limit on Buck 4. Note that OC_LEV_B0...B5 should have the same value. 00 = 1.5 A 01 = 2.0 A 10 = 2.5 A 11 = 3.0 A
5:0	Reserved	R/W	01 0001	

7.6.9 BUCK5_CTRL

Address: 0x0C

D7	D6	D5	D4	D3	D2	D1	D0
OC_LEV_B5[1:0]		Reserved					

Bits	Field	Type	Default	Description
7:6	OC_LEV_B5[1:0]	R/W	11	Inductor positive current limit on Buck 5. Note that OC_LEV_B0...B5 should have the same value. 00 = 1.5 A 01 = 2.0 A 10 = 2.5 A 11 = 3.0 A
5:0	Reserved	R/W	01 0001	

7.6.10 FLAGS_0

Address: 0x0D

D7	D6	D5	D4	D3	D2	D1	D0
Reserved					nPG_B0	TEMP[1:0]	

Bits	Field	Type	Default	Description
7:3	Reserved	R/W	X XXXX	
2	nPG_B0	R/W	0	Flag Bit (1) Power good fault flag for V_{OUT} rail 1 = Power fault detected 0 = Power good
1:0	TEMP[1:0]	R	00	indicates the die temperature as follows: 00: die temperature lower than 85ºC 01: 85ºC ≤ die temperature < 120ºC 10: 120ºC ≤ die temperature < 150ºC 11: die temperature 150ºC or higher

(1) The flag bit can be cleared only by writing a zero to the associated register bit or power cycling the device (V_{VIOSYS} to LOW). Reading or RESET does not clear the flag bits. After clearing, the nPG fault flag will be raised again '1' if the fault condition persists. Any unmasked flag bit High will cause the interrupt to be asserted on the INT pin. The INT pin will be pulled Low until all the unmasked flags are clear again.

7.6.11 FLAGS_1

Address: 0x0E

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D7	D6	D5	D4	D3	D2	D1	D0
Reserved		I_LOAD_READY	UVLO	T_WARNING	THSD	OVP	SCP

Bits	Field	Type	Default	Description
7:6	Reserved	R/W	00	
5	I_LOAD_READY	R/W	0	Flag Bit(1) 1 = Buck load current measurement data ready 0 = Buck load current measurement data not ready
4	UVLO	R/W	0	Flag Bit (1) 1= Input undervoltage lockout (UVLO): Input voltage sagged below UVLO threshold. 0 = No UVLO
3	T_WARNING	R/W	0	Flag Bit (1) 1= Thermal warning: The IC temperature exceeds 120°C, in advance of the thermal shutdown protection. 0 = No thermal warning
2	THSD	R/W	0	Flag Bit (1) 1 = Thermal shutdown event detected 0 = No thermal shutdown
1	OVP	R/W	0	Flag Bit (1) 1= Indicates overvoltage protection (OVP) circuit activation. 0 = No OVP event. The OVP circuitry monitors VDDA5V power input.
0	SCP	R/W	0	Flag Bit (1) 1= Indicates short-circuit protection (SCP) circuit activation. The bit is activated when a short-circuit condition is detectedon output rail. 0 = No SCP event

(1) The flag bit(s) can be cleared only by writing a zero to the associated register bit(s) or power cycling the device (V_{VIOSYS} to LOW). Reading or RESET does not clear the flag bits. After clearing, the OVP, SCP fault flag(s) will be raised again '1' if the fault condition persists. The THSD flag will remain '0' after clear, even though the fault condition persists. Any unmasked flag bit High will cause the interrupt to be asserted on the INT pin. The INT pin will be pulled Low until all the unmasked flags are clear again.

7.6.12 INT_MASK_0

Address: 0x0F

D7	D6	D5	D4	D3	D2	D1	D0
Reserved					MASK_nPG_B0	MASK_OVP	MASK_SCP

Bits	Field	Type	Default	Description
7:3	Reserved	R/W	1 1111	
2	MASK_nPG_B0	R/W	0	Interrupt mask for power good fault flag 1 = nPG does not set interrupt. 0 = nPG sets interrupt, when triggered.
1	MASK_OVP	R/W	0	Interrupt mask for Overvoltage Protection (OVP) fault flag 1 = OVP does not set interrupt. 0 = OVP sets interrupt, when triggered.
0	MASK_SCP	R/W	0	Interrupt mask for short-circuit protection SCP fault flag 1 = SCP does not set interrupt. 0 = SCP sets interrupt, when triggered.

7.6.13 GENERAL

Address: 0x10

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		EN_SS	Reserved	DIS_DIF_B0		SLP_POL	LP_EN

Bits	Field	Type	Default	Description
7:6	Reserved	R/W	00	
5	EN_SS	R/W	0	Spread Spectrum 1 = Spread Spectrum enabled 0 = Spread Spectrum disabled
4	Reserved	R/W	0	
3	DIS_DIF_B0	R/W	0	Disable Differential-to-single-ended amplifier 1 = Differential amplifier disabled 0 = Differential amplifier enabled
2		R/W	0	
1	SLP_POL	R/W	0	Sets the polarity of the NSLP pin 1 = NSLP is active high 0 = NSLP is active low
0	LP_EN	R/W	1	1 = allows Low-Power PFM mode. In order to reduce power consumption under low load conditions, the unit will automatically switch off unused internal blocks. 0 = Low-Power mode not allowed

7.6.14 RESET

Address: 0x11

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							SW_RESET

Bits	Field	Type	Default	Description
7:1	Reserved	R/W	000 0000	
0	SW_RESET	R/W	0	Writing this bit with '1' and '0', in this order, will reset the registers to the default values. If NRST is still kept HIGH, the converter output(s) will be regulated to the programmed register values. If a full POR reset is required V_{VIOSYS} must be pulled low. The fault flags are persistent over SW-reset.

7.6.15 DELAY_BUCK0

Address: 0x12

D7	D6	D5	D4	D3	D2	D1	D0
DELAY_B0							

Bits	Field	Type	Default	Description
7:0	DELAY_B0	R/W	0000 0000	Master delay Sets the delay time from when NRST is asserted to when the V_{OUT} rail is enabled. Sets the delay time from when NRST is de-asserted to when the V_{OUT} rail is disabled. DELAY = DELAY_B0 * 100 µs If DELAY_B0 = FFh, supply is never enabled. (1)

(1) If this register is set to FFh when the converter is already started, it will cause an immediate power down of the converter.

7.6.16 CHIP_ID

Address: 0x18

D7	D6	D5	D4	D3	D2	D1	D0
DEVICE	OTP_REV					DIE_REV	

Bits	Field	Type	Default	Description
7	DEVICE	R	1	DEVICE Contains Device ID
6:2	OTP_REV	R	0 0001	OTP_REV Contains OTP Version ID

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Bits	Field	Type	Default	Description
1:0	DIE_REV	R	00	DIE_REV Contains Revision ID

7.6.17 PFM_LEV_B0

Address: 0x19

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	PFM_ENTRY_B0[2:0]			Reserved	PFM_EXIT_B0[2:0]		

Bits	Field	Type	Default	Description
7	Reserved	R/W	0	
6:4	PFM_ENTRY_B0	R/W		PFM_ENTRY_B0 (1) Sets the target PFM entry level for Buck 0. The final PWM-to-PFM switchover current varies slightly and is dependant on the output voltage, input voltage and the inductor current level. 000 = 50 mA 001 = 75 mA 010 = 100 mA 011 = 125 mA 100 = 175 mA 101 = 225 mA 110 = 275 mA 111 = 325 mA
3	Reserved	R/W	0	
2:0	PFM_EXIT_B0	R/W	101	PFM_EXIT_B0 (1) Sets the target PFM exit level for Buck 0. The final PFM-to-PWM switchover current varies slightly and is dependant on the output voltage, input voltage and the inductor current level. 000 = 100 mA 001 = 125 mA 010 = 150 mA 011 = 175 mA 100 = 225 mA 101 = 275 mA 110 = 325 mA 111 = 375 mA

(1) For proper operation, the PFM exit current level should be at least 50 mA higher than the PFM entry current level.

7.6.18 PHASE_LEV_B0

Address: 0x1F

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	ADD_PH_B0[2:0]			Reserved	SHED_PH_B0[2:0]		

Bits	Field	Type	Default	Description
7	Reserved	R/W	0	
6:4	ADD_PH_B0	R/W	100	ADD_PH_B0(1) Sets the level on which a phase is added. 000 = 0.3 A * No. of Active Phases 001 = 0.4 A * No. of Active Phases 010 = 0.5 A * No. of Active Phases 011 = 0.6 A * No. of Active Phases 100 = 0.7 A * No. of Active Phases 101 = 0.8 A * No. of Active Phases 110 = 0.9 A * No. of Active Phases 111 = 1.0 A * No. of Active Phases
3	Reserved	R/W	0	

(1) ADD_PH_B0 and SHED_PH_B0 values must be chosen so that the resulting hysteresis is a minimum of 100 mA and ADD_PH_B0 > SHED_PH_B0.

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Bits	Field	Type	Default	Description
2:0	SHED_PH_B0	R/W	010	SHED_PH_B0 (1) Sets the level of phase shedding. 000 = 0.3 A * No. of Active Phases 001 = 0.4 A * No. of Active Phases 010 = 0.5 A * No. of Active Phases 011 = 0.6 A * No. of Active Phases 100 = 0.7 A * No. of Active Phases 101 = 0.8 A * No. of Active Phases 110 = 0.9 A * No. of Active Phases 111 = 1.0 A * No. of Active Phases

7.6.19 SEL_I_LOAD

Address: 0x21

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	BUCK_LOAD_CURR[10:8]			Reserved	LOAD_CURRENT_SOURCE[2:0]		

Bits	Field	Type	Default	Description
7	Reserved	R/W	0	
6:4	BUCK_LOAD_ CURR[10:8]	R	000	BUCK_LOAD_CURR This register reports 3 MSB bits of the magnitude of the average load current of the selected Buck Converter. See LOAD_CURR register.
3	Reserved	R/W	0	
2:0	LOAD_CURRENT_ SOURCE[2:0]	R/W	000	LOAD_CURRENT_SOURCE These bits are used for choosing the Buck Converter whose load current will be measured. 000 = Converter 0 load current will be measured. 001 = Converter 1 load current will be measured. 010 = Converter 2 load current will be measured. 011 = Converter 3 load current will be measured. 100 = Converter 4 load current will be measured. 101 = Converter 5 load current will be measured. 110 = Master total load current will be measured.

7.6.20 LOAD_CURR

Address: 0x22

D7	D6	D5	D4	D3	D2	D1	D0
BUCK_LOAD_CURR[7:0]							

Bits	Field	Type	Default	Description
7:0	BUCK_LOAD_ CURR[7:0]	R	0000 0000	BUCK_LOAD_CURR This register reports 8 LSB bits of the magnitude of the average load current of the selected Buck Converter. The value is reported with a resolution of 10 mA per LSB and 20A max current. Three MSB bits are reported by SEL_I_LOAD.BUCK_LOAD_CURR[10:8] bits, see SEL_I_LOAD. The current reported is an average over the last 5 milliseconds. The host system has read-only access to this register. This register is cleared to 0 on all resets. 000 0000 0000 Load current lower than 10 mA 000 0000 0001 10 mA ≤ Load current < 20 mA ... 111 1111 1110 20460 mA ≤ Load current < 20470 mA 111 1111 1111 Load current 20470 mA or higher. Note: Not production tested. Typical values for reference only.

7.6.21 INT_MASK_2

Address: 0x2E

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D7	D6	D5	D4	D3	D2	D1	D0
Reserved				MASK_ILOAD_READY	MASK_UVLO	MASK_TWARNING	MASK_TEMP

Bits	Field	Type	Default	Description
7:4	Reserved	R/W	0000	
3	MASK_ILOAD_READY	R/W	1	Interrupt mask for load current measurement flag 1 = FLAGS_1.I_LOAD_READY does not set interrupt. 0 = FLAGS_1.I_LOAD_READY sets interrupt.
2	MASK_UVLO	R/W	0	Interrupt mask for undervoltage lock-out flag 1 = FLAGS_1.UVLO does not set interrupt. 0 = FLAGS_1.UVLO sets interrupt, when triggered.
1	MASK_TWARNING	R/W	1	Interrupt mask for thermal warning flag 1 = FLAGS_1.T_WARNING does not set interrupt. 0 = FLAGS_1.T_WARNING sets interrupt, when triggered.
0	MASK_TEMP	R/W	1	Interrupt mask for die temperature flag bits 1 = FLAGS_0.TEMP[1:0] value change does not set interrupt. 0 = FLAGS_0.TEMP[1:0] value change sets interrupt.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP8755 is a multi-phase step-down converter with 6 switcher cores bundled together.

8.2 Typical Application

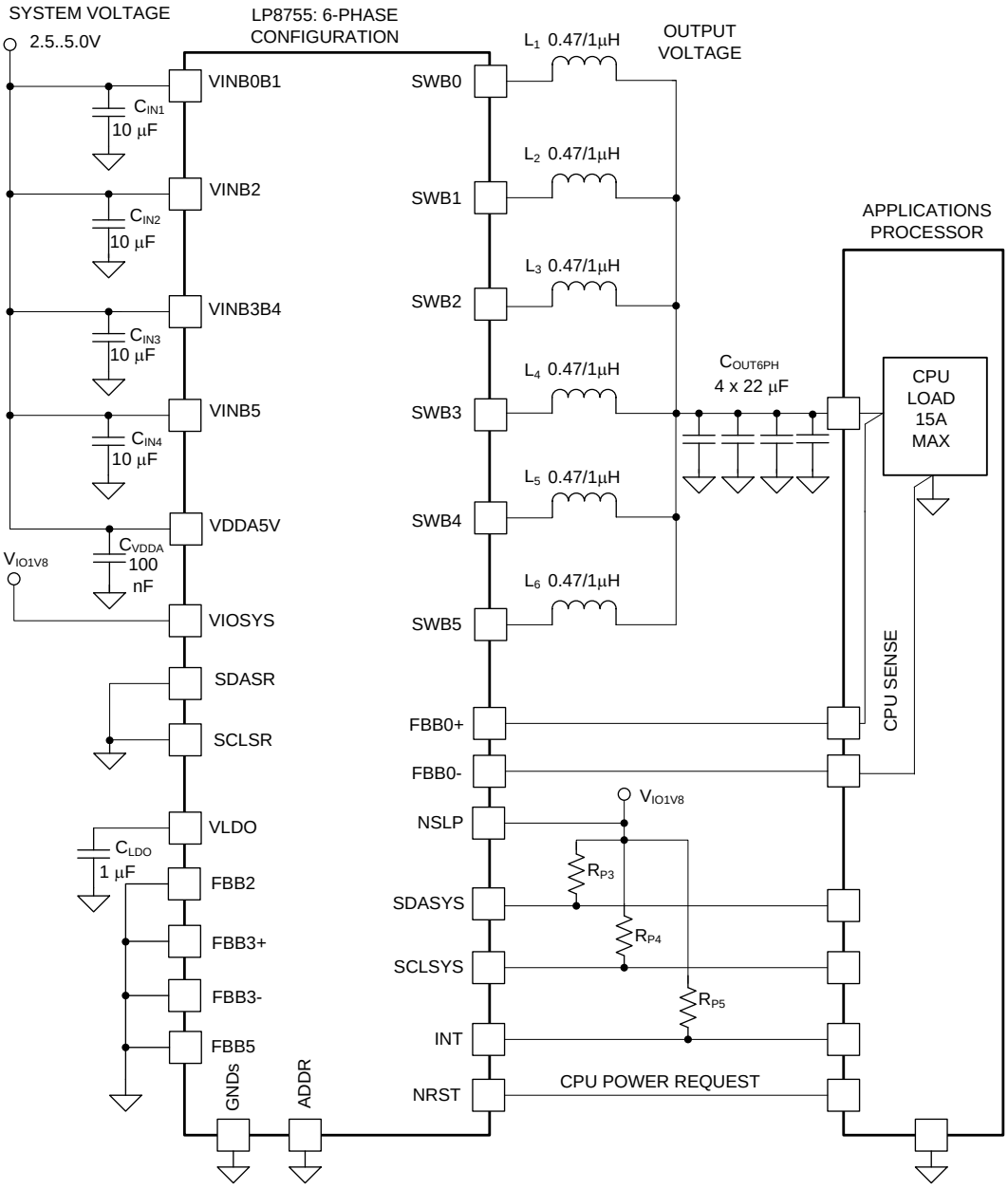

Figure 23. Six-Phase Configuration Scheme

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Typical Application (continued)

8.2.1 Design Requirements

Table 6 shows requirements for 6-phase configuration.

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 5 V
Output voltage	1.1 V
Converter operation mode	Forced PWM
Maximum load current	15 A
Inductor current limit	3 A

8.2.2 Detailed Design Procedure

The performance of the LP8755 device depends greatly on the care taken in designing the Printed Circuit Board (PCB). The use of low inductance and low serial resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the IC and between the power and ground pins to support high peak currents being drawn from System Power Rail during turn-on of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance and capacitance can easily become the performance limiting items. The separate power pins VINBXX are not connected together internally. The VINBXX power connections shall be connected together outside the package using power plane construction.

8.2.2.1 Inductor Selection

The DC bias current characteristics of inductors must be considered. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. (Please request DC bias curves from the manufacturer as part of the inductor selection process.) Minimum effective value of inductance to ensure good performance is 0.25 µH at 3.2 A (Default I_{LIMITP} typical) bias current over the inductor's operating temperature range. The inductor's DC resistance should be less than 0.05 Ω for good efficiency at high-current condition. The inductor AC loss (resistance) also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle load. Table 7 lists suggested inductors and suppliers. Shielded inductors radiate less noise and are preferable.

Table 7. Suggested Inductor Selection

ITEM	MODEL	VENDOR	DIMENSIONS LXWXH (mm)	D.C.R (mΩ) MAX
L1 to L6; Step-down converter inductor 0.47 µH	XFL4015-471ME_ (1) LQH32PNR47NN0 (2) DFE252012 R47 (3) DFE201612C R47N (4) LQM2MPNR47MGH (4)	Coilcraft Murata TOKO TOKO Murata	4 .0 x 4.0 x 1.5 3.2 x 2.5 x 1.55 2.5 x 2 x 1.2 2.0 x 1.6 x 1.2 2.0 x 1.6 x 1.0	8.4 30 ± 20 % 39 50 46
L1 to L6; Step-down converter inductor 0.68 µH	DFE322512 R68	TOKO	3.2 x 2.5 x 1.2	37
L1 to L6; Step-down converter inductor 1 µH	DFE322512 1R0	TOKO	3.2 x 2.5 x 1.2	45

(1) Best efficiency.
(2) Good balance between size and efficiency.
(3) Satisfactory compromise between size and efficiency.
(4) Applications for which solution size is critical, efficiency compromised on very high loads.

8.2.2.2 Input Capacitor Selection

A ceramic input capacitor of 10 µF, 10 V is sufficient for most applications. Place the input capacitor as close as possible to the VINBXX pin and GND pin of the device. A larger value or higher voltage rating may be used to improve input voltage filtering. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0402. Minimum effective input capacitance to ensure good performance is 2.5 µF at maximum input voltage DC bias including tolerances and over ambient temp range, assuming that there is at least 22 µF of additional capacitance common for all the power input pins on the system power rail.

The input filter capacitor supplies current to the PFET (high-side) switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low equivalent series resistance (ESR) provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating.

For additional noise immunity, adding a high-frequency decoupling capacitor of 100 nF to 1 µF between VDDA5V pin and GND is recommended.

Table 8. Suggested Input Capacitors (X5R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	VOLTAGE RATING
Murata	GRM188R60J106ME84	10 µF (20%)	0603	6.3 V
TDK	C1608X5R1A106KT	10 µF (10%)	0603	10 V
Taiyo Yuden	LMK107BJ106MALTD	10 µF (20%)	0603	10 V
Samsung	CL10A226MP8NUNE	22 µF (20%)	0603	10 V

8.2.2.3 Output Capacitor Selection

Use ceramic capacitor, X7R or X5R types; do not use Y5V. DC bias voltage characteristics of ceramic capacitors must be considered. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them as part of the capacitor selection process. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions. Minimum effective output capacitance to ensure good performance in 6-phase configuration is 30 µF at the output voltage DC bias including tolerances and over ambient temp range.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its R_{ESR}. The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the switching frequency of the part.

A higher output capacitance improves the load step behavior and reduces the output voltage ripple as well as decreasing the PFM switching frequency. For most 6-phase applications 4 x 22-µF 0603 capacitors for C_{OUT} is suitable. Although the converter's loop compensation can be programmed to adapt to virtually several hundreds of microfarads C_{OUT}, an effective C_{OUT} less than 120 µF is preferred -- there is not necessarily any benefit to having a C_{OUT} higher than 120 µF. Note that the output capacitor may be the limiting factor in the output voltage ramp, especially for very large (> 100 µF) output capacitors. For large output capacitors, the output voltage might be slower than the programmed ramp rate at voltage transitions, because of the higher energy stored on the output capacitance. Also at start-up, the time required to charge the output capacitor to target value might be longer. At shutdown, if the output capacitor is discharged by the internal discharge resistor, more time is required to settle V_{OUT} down as a consequence of the increased time constant.

Table 9. Suggested Output Capacitor

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	VOLTAGE RATING
Samsung	CL10A226MP8NUNE	22 µF (20%)	0603	10 V

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8.2.2.4 LDO Capacitor Selection

A ceramic low ESR 1-µF capacitor should be connected between the VLDO and GNDA pins.

Table 10. Suggested LDO Capacitor

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	VOLTAGE RATING
Samsung	CL03A105MQ3CSNH	1 µF (20%)	0201	6.3 V

8.2.2.5 VIOSYS Capacitor Selection

Adding a ceramic low ESR 1-µF capacitor between the VIOSYS pin and GND is recommended. If V_{VIOSYS} signal is low noisy the capacitor is not required.

8.2.3 Application Curves

Unless otherwise specified: V_{VDDA5V} = V_{VINBXX} = 3.7 V, V_{OUT} = 1.1 V, T_A = 25°C

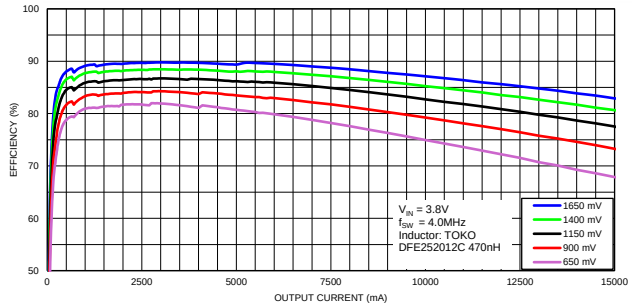

Figure 24. Efficiency vs Load Current in PWM Mode; V_{OUT} Settings = 650 mV, 950 mV, 1150 mV, 1400 mV and 1650 mV

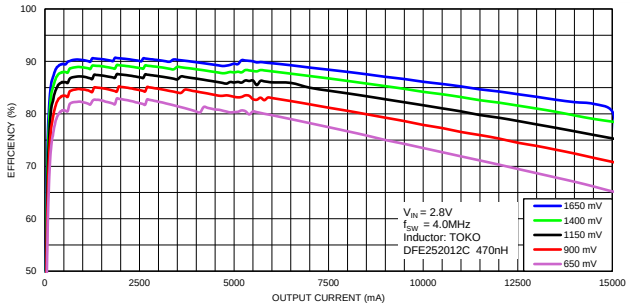

Figure 25. Efficiency vs Load Current in PWM Mode; V_{OUT} Settings = 650 mV, 950 mV, 1150 mV, 1400 mV and 1650 mV

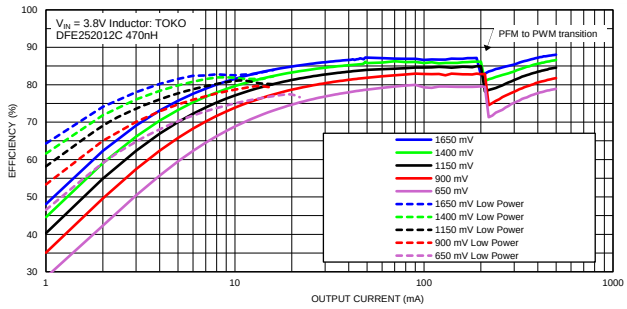

Figure 26. Light Load Efficiency, PFM and Low Power Mode Enabled; V_{OUT} Settings = 650 mV, 950 mV, 1150 mV, 1400 mV and 1650 mV. PFM_EXIT_B0[2:0] = 100b (225 mA)

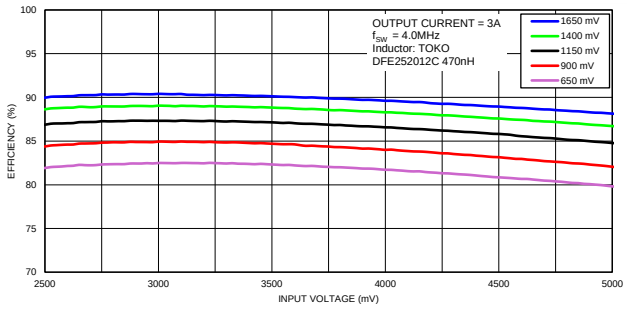

Figure 27. Efficiency vs Input Voltage in PWM Mode; V_{OUT} Settings = 650 mV, 950 mV, 1150 mV, 1400 mV and 1650 mV

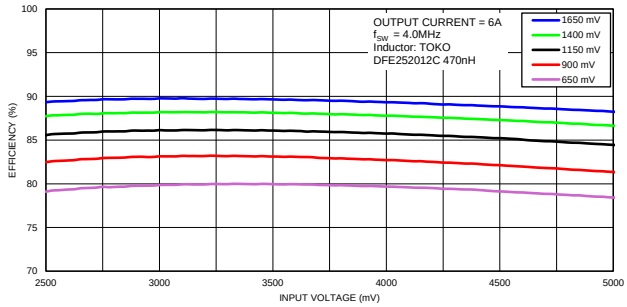

Figure 28. Efficiency vs Input Voltage in PWM Mode; V_{OUT} Settings = 650 mV, 950 mV, 1150 mV, 1400 mV and 1650 mV

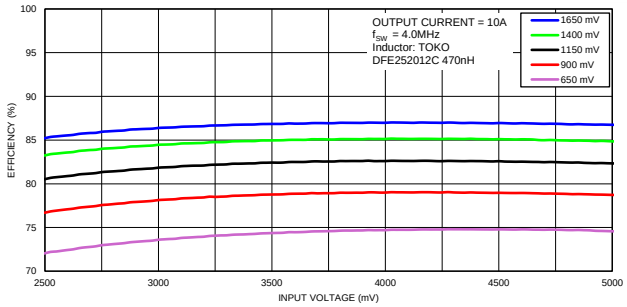

Figure 29. Efficiency vs Input Voltage in PWM Mode; V_{OUT} Settings = 650 mV, 950 mV, 1150 mV, 1400 mV and 1650 mV

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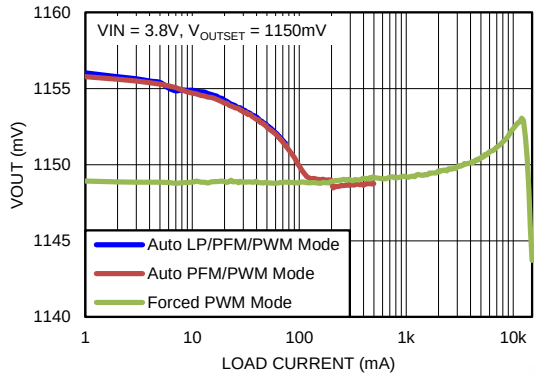


Figure 30. Output Voltage vs Load Current in Different Modes

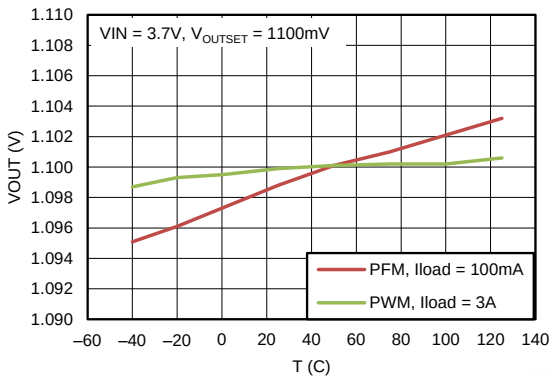


Figure 31. Output Voltage vs Temperature

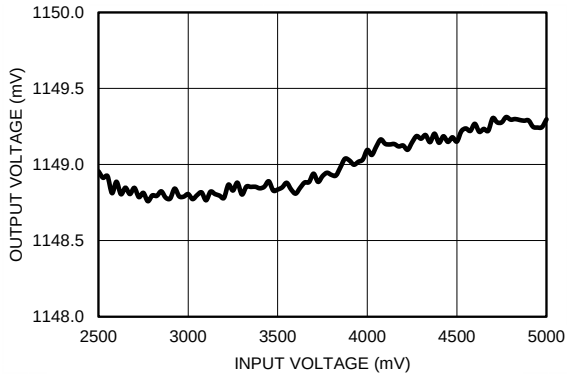


Figure 32. Line Regulation; I_{LOAD} = 1 A; V_{OUTSET} = 1150 mV

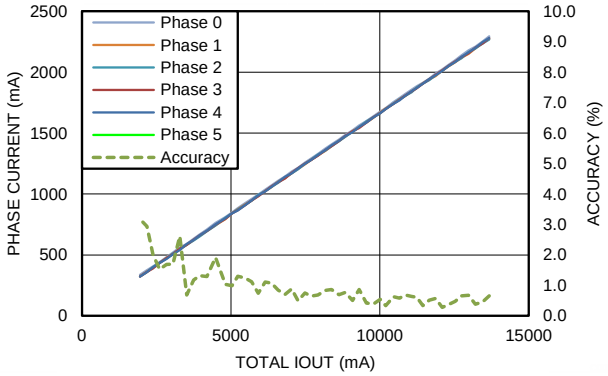


Figure 33. Phase Currents and Current Balancing Accuracy, 6 Phases Active (Currents measured by LP8755)

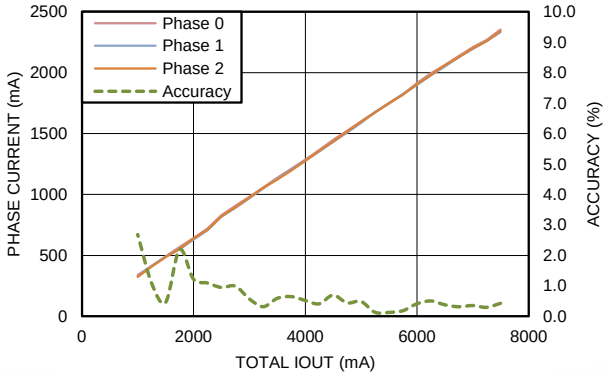


Figure 34. Phase Currents and Current Balancing Accuracy, 3 Phases Active (Currents measured by LP8755)

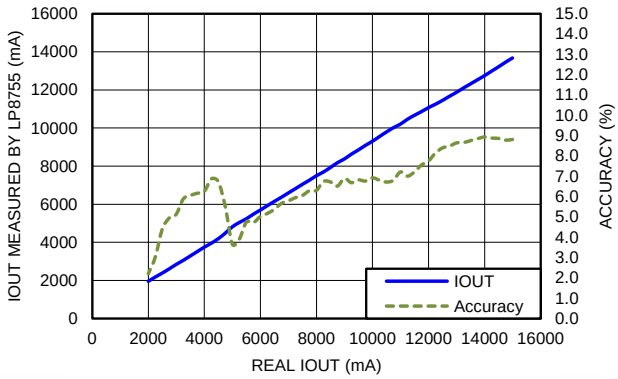


Figure 35. Load Current Measured by LP8755 vs Real Load Current, 6 Phases Active

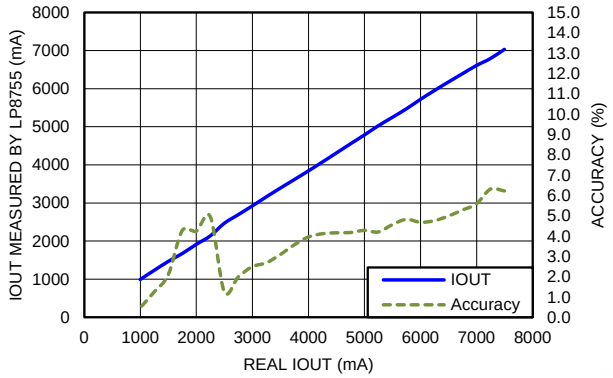
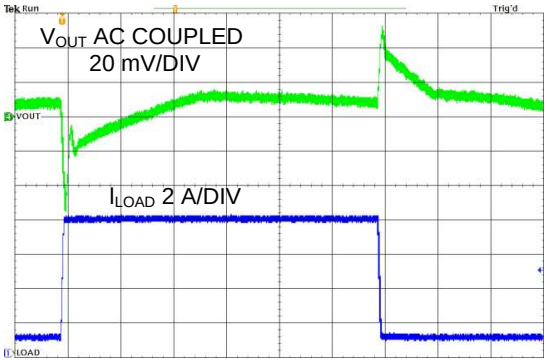
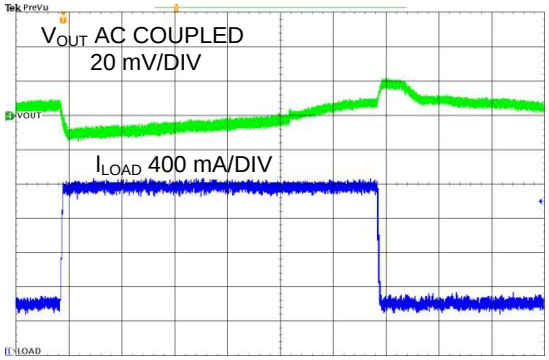


Figure 36. Load Current Measured by LP8755 vs Real Load Current, 3 Phases Active



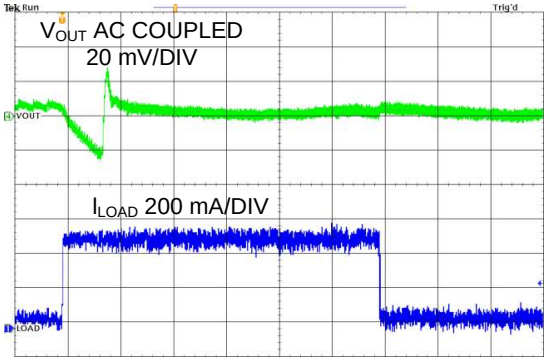
TIME 10 µs/DIV

Figure 37. Transient Load Step Response; PWM mode, I_{OUT} 1 A → 8 A → 1 A, t_{RISE} = t_{FALL}= 400 ns



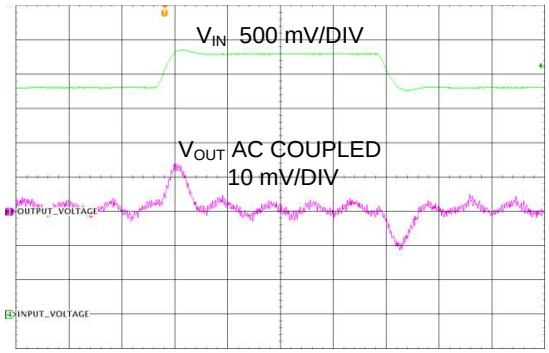
TIME 10 µs/DIV

Figure 38. Transient Load Step Response; PWM mode, I_{OUT} 0.6 A → 2 A → 0.6 A, t_{RISE} = t_{FALL}= 400 ns



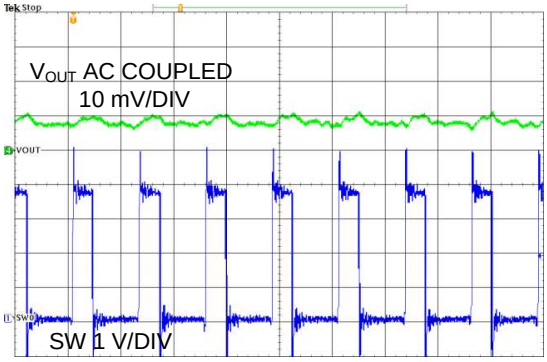
TIME 10 µs/DIV

Figure 39. Transient Load Step Response; AUTO mode, I_{OUT} 0.5 mA → 500 mA → 0.5 mA, t_{RISE} = t_{FALL}= 100 ns



TIME 40 µs/DIV

Figure 40. Transient Line Response; I_{OUT} = 2000 mA DC



TIME 200 ns/DIV

Figure 41. Output Voltage Ripple, PWM Mode. I_{OUT} = 200 mA; One Phase Active

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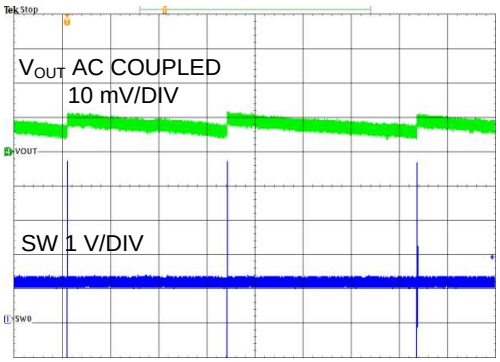


Figure 42. Output Voltage Ripple, PFM Mode. I_{OUT} = 100 µA

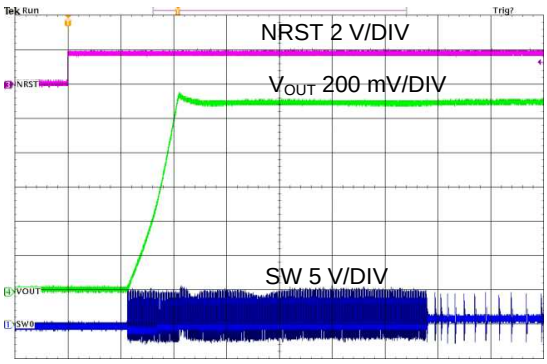


Figure 43. Start-up with NRST, No Load

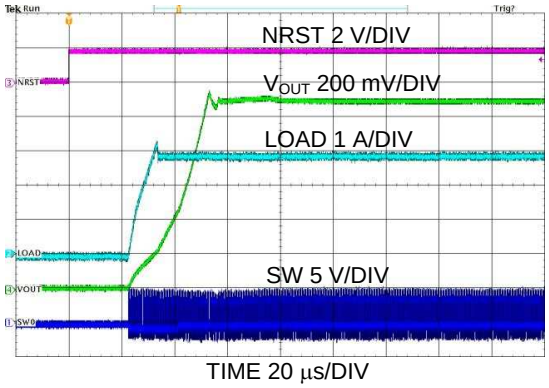


Figure 44. Start-up with NRST, 3-A Load

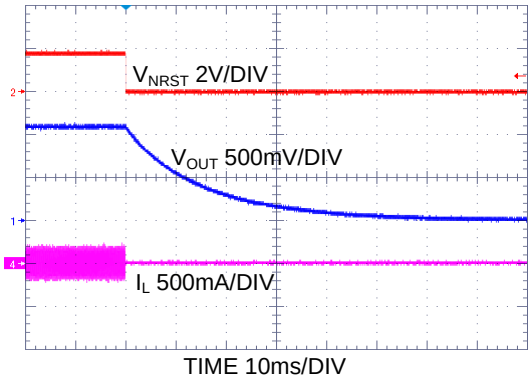


Figure 45. Shutdown with NRST, V_{IN} = 3.7 V, V_{OUT} = 1.1 V, No Load, Forced PWM

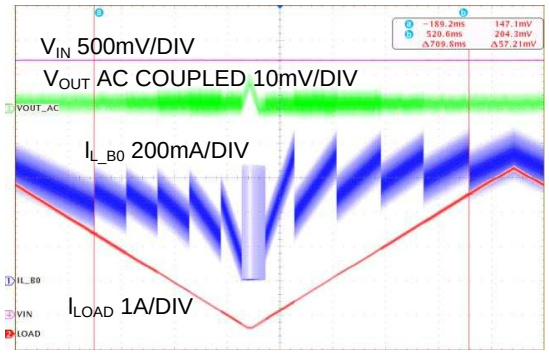


Figure 46. Load ramp 4.5 A → 0 A → 4.5 A

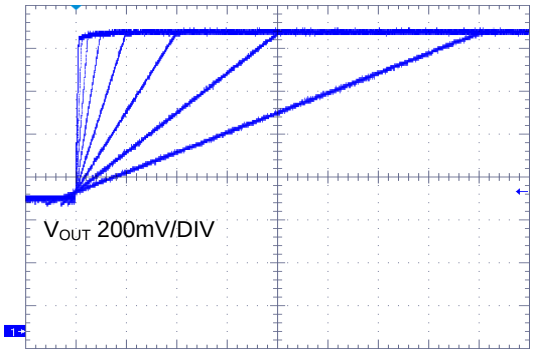
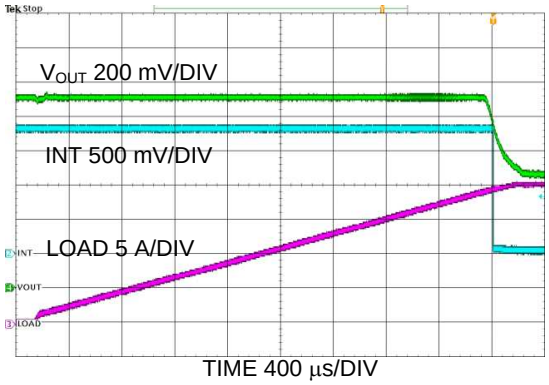
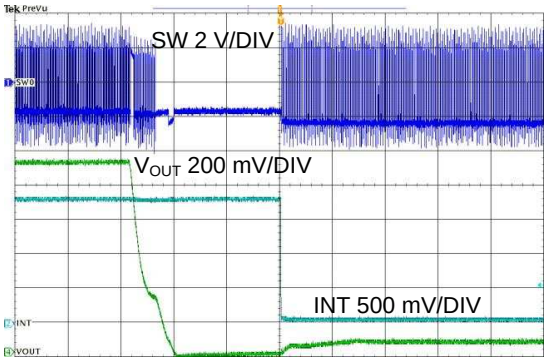


Figure 47. V_{OUT} Transition from 0.6 V to 1.4 V with Different Ramp Settings, V_{IN} = 3.7 V



TIME 400 µs/DIV

Figure 48. Interrupt Line Going Low with Not Power Good Activation



TIME 10 µs/DIV

Figure 49. Metallic Short Applied at V_{OUT}

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9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5 V and 5 V. This input supply should be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail should be low enough that the input current transient does not cause too high drop in the LP8755 supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the LP8755 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The high frequency and large switching currents of the LP8755 make the choice of layout important. Good power supply results will only occur when care is given to proper design and layout. Bad layout will affect noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamps to 10 A and over, good power-supply layout is more challenging than for most general PCB design. The following steps should be used as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range:

1. Place C_{IN} as close as possible to the VINBXX pin and the GND pin. Route the V_{IN} trace wide and thick to avoid IR drops. The trace between the input capacitor's positive node and LP8755's VINBXX pin(s) as well as the trace between the input capacitor's negative node and power GND pin(s) must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter.
2. The output filter for each buck, consisting of C_{OUT} and L, converts the switching signal at SW to the noiseless output voltage. For optimal EMI behavior, it should be placed as close as possible to the device, keeping the switch node small. Route the traces between the LP8755's output capacitors and the load's input capacitors direct and wide to avoid losses due to the IR drop.
3. Input for analog blocks (VDDA5V and GNDA) should be isolated from noisy signals. Connect VDDA5V directly to a quiet system voltage node and GNDA to a quiet ground point where no IR drop occurs. For additional noise immunity, adding a high-frequency decoupling capacitor of 100 nF to 1 µF is recommended. Place the decoupling capacitor as close to the VDDA5V pin as possible. VDDA5V trace is low current, so the trace width does not need to be optimized.
4. If the processor load supports voltage remote sensing, connect the LP8755 feedback pins FBBXX to the respective sense pins on the processor. The sense lines are susceptible to noise. They must be kept away from noisy signals such as GNDBXX, V_{IN}, and SW, as well as high bandwidth signals such as the I^2C. Avoid both capacitive as well as inductive coupling by keeping the sense lines short, direct, and close to each other. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible. Running the signal as a differential pair is recommended.
5. GNDBXX, VIN, and SW should be routed on thick layers. They must not surround inner signal layers which are not able to withstand interference from noisy GNDBXX, V_{IN}, and SW. This can create noise coupling to inner signal layers.

Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide power traces come with the ability to sink dissipated heat. This can be improved further on multi-layer PCB designs with vias to different planes. This results in reduced junction-to-ambient ($R_{\theta JA}$) and junction-to-board ($R_{\theta JB}$) thermal resistances, thereby reducing the device junction temperature, T_J. It's strongly recommended to perform a careful system-level 2D or full 3D dynamic thermal analysis at the beginning of the product design process, using a thermal modeling analysis software.

10.2 Layout Example

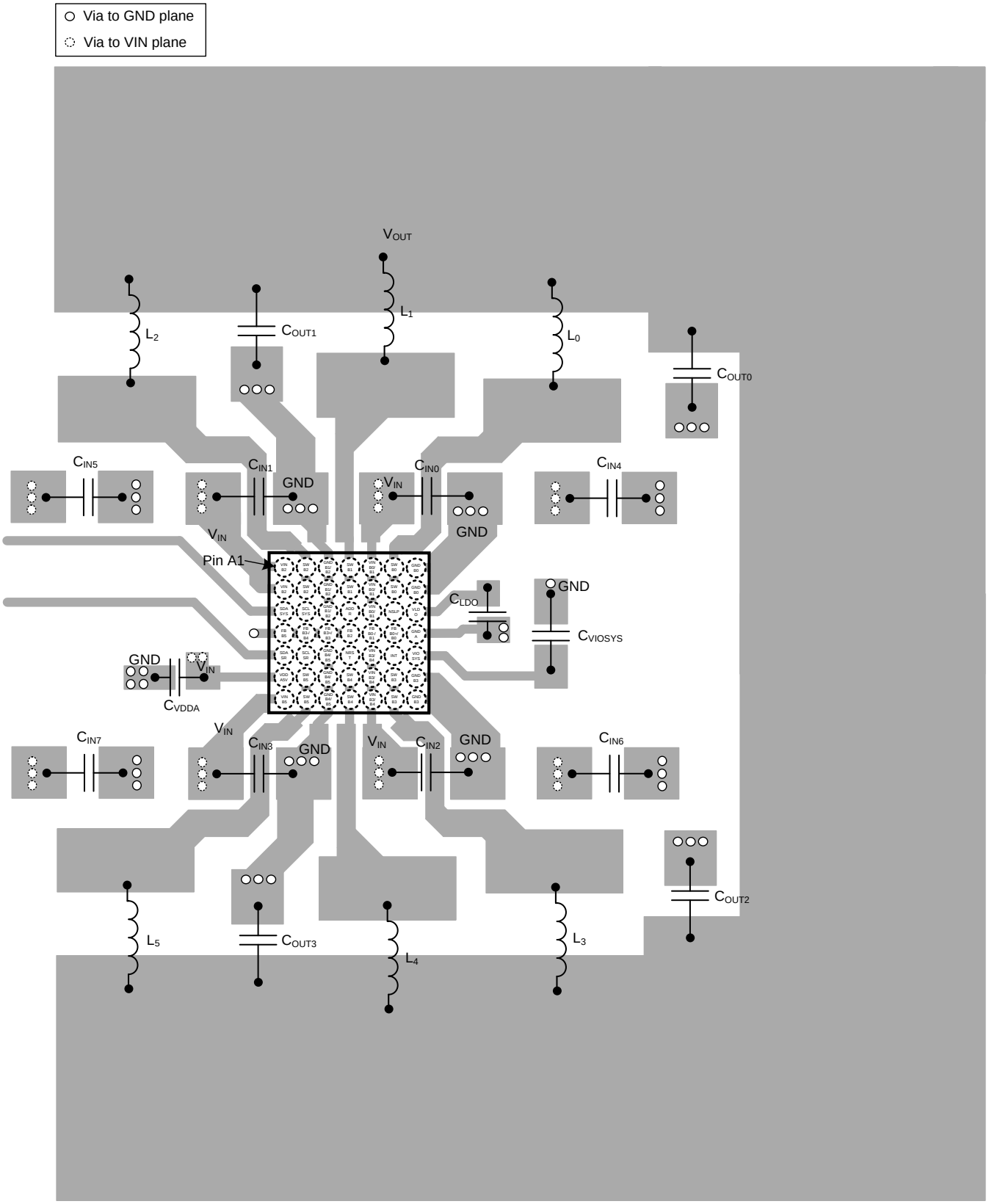

Figure 50. LP8755 Board Layout

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments Application Note *DSBGA Wafer-Level Chip-Scale Package* (SNVA009).

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8755KME/NOPB	NRND	DSBGA	YFQ	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	8755	
LP8755KMX/NOPB	NRND	DSBGA	YFQ	49	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	8755	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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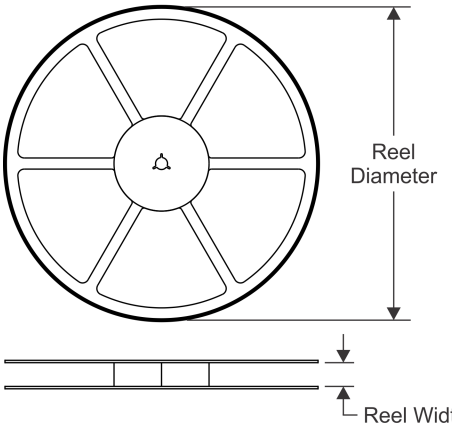
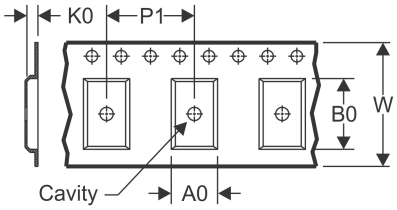
TAPE AND REEL INFORMATION

REEL DIMENSIONS

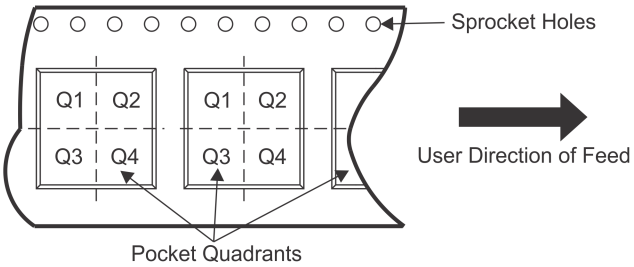


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

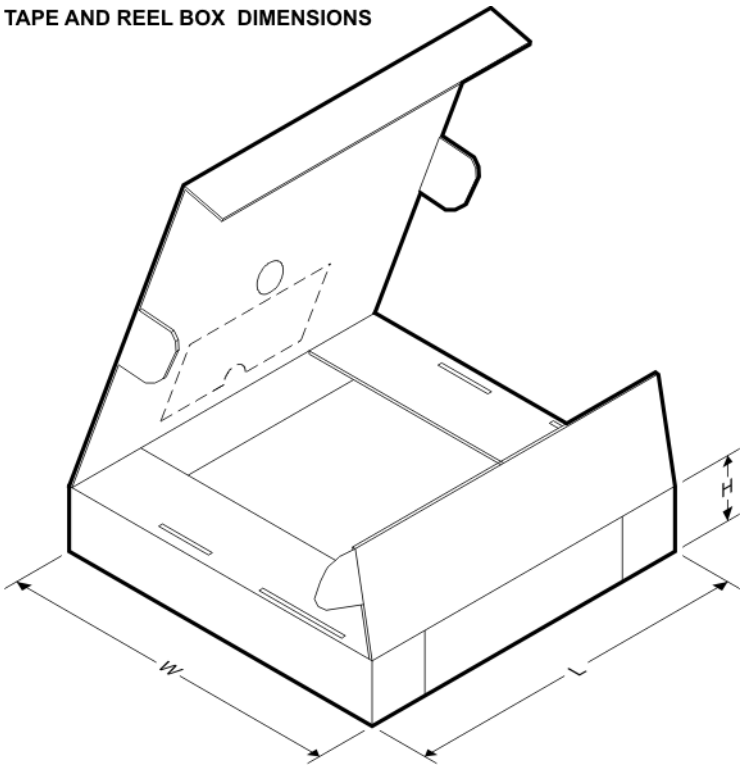
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8755KME/NOPB	DSBGA	YFQ	49	250	180.0	13.0	3.06	3.2	0.71	8.0	12.0	Q1
LP8755KMX/NOPB	DSBGA	YFQ	49	1000	180.0	13.0	3.06	3.2	0.71	8.0	12.0	Q1

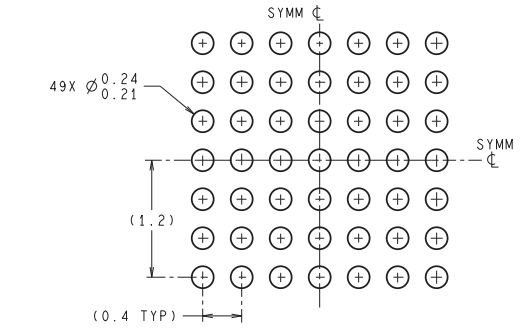
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

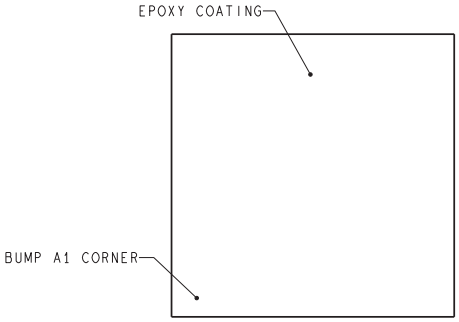
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8755KME/NOPB	DSBGA	YFQ	49	250	200.0	230.0	25.0
LP8755KMX/NOPB	DSBGA	YFQ	49	1000	200.0	230.0	25.0

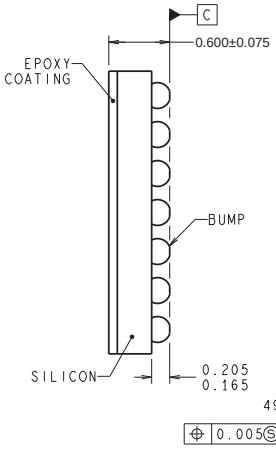
YFQ0049

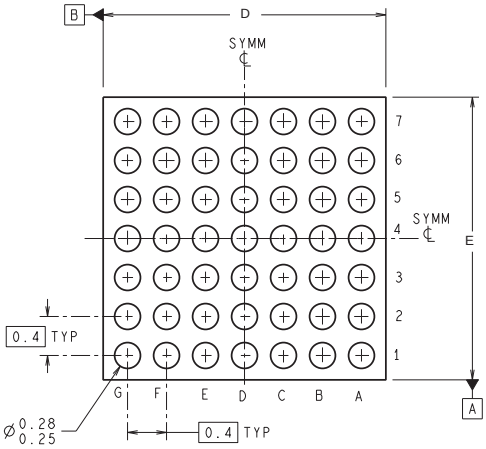


LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







TMD49XXX (Rev A)

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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